SPS001

TMS5220C

This is coming to the TMS5200, which is used in the 99/4 speech synthesizer.

Speech Products
Preliminary Data Manual

TEXAS INSTRUMENTS

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SPSS001

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SECTION 1

INTRODUCTION

1.1 SCOPE

This data manual will detail the functional characteristics of the TMS5220C voice synthesis Processor (VSP). Included will be a brief discussion of the Linear Predictive Coding (LPC) method of encoding speech. It is recommended that the user also consult the data manual(s) for the type of ROM voice synthesis memory (VSM) being used for a particular application.

1.2 DEVICE FUNCTION

The TMS5220C VSP uses a 10 pole filter and Linear Predictive Coding to produce verbal responses from information provided by a CPU. The host accesses speech data from memory. These speech data are then sent to yhe VSP for decoding and synthesis at a predetermined frame rate. An interpolation is performed before the synthesis for better smoothing in output speech. During the synthesis, a 10-pole lattice filter is used to model the human vocal tract. After speech data are generated by the filter, a digital to analog converter is used to produce an amplitude modulated waveform ready for amplification.

The synthesizer may also obtain speech data by direct serial access of a VSM. TI offers two types on memory devices: the TMS6100 and TMS6125. For more information concerning these devices and vocabulary generation contact your TI representative or Texas Instruments Regional Technology Center. For further information see the listing on the back of this manual.

Following is a block diagram of the TMS5220C.

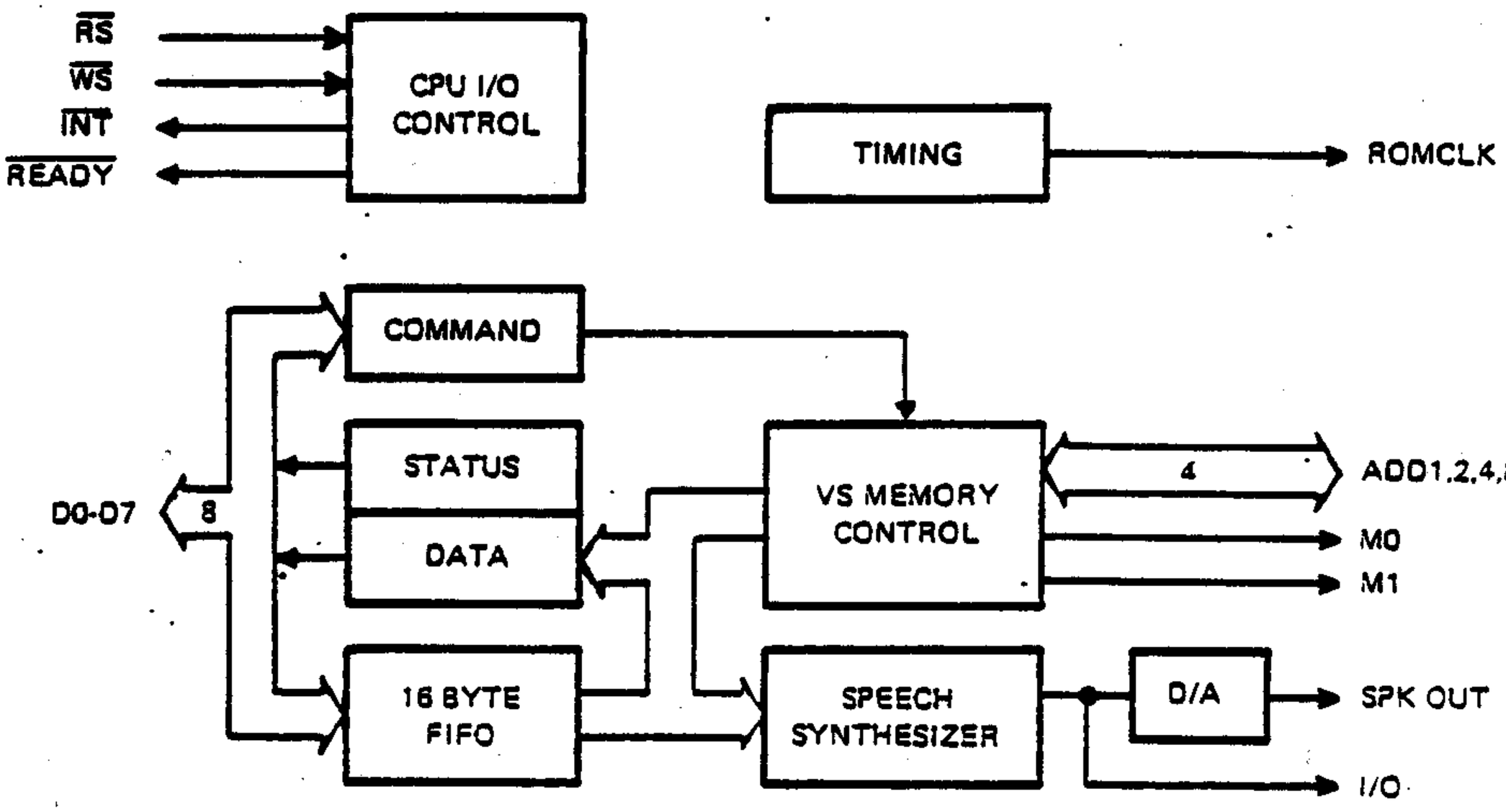


FIGURE 1.1. SYNTHESIZER BLOCK DIAGRAM

1.3 KEY FEATURES

The TMS5220C incorporates the following key features to insure low cost high quality speech from a microcomputer system.

- Low-Data-Rate LPC encoding
- Variable-frame-rate
- Low-Cost P-channel MOS technology
- Interrupt-based service requests
- TTL compatible*
- Optional package size

* Refer to the electrical specification for TTL compatibility

SECTION 2

DEVICE DESCRIPTION

2.1 PIN ASSIGNMENTS AND FUNCTIONS

The following table and figure present a guide of the external connections for the TMS5220C.

TABLE 2-1. PIN ASSIGNMENTS AND FUNCTIONS

PIN	NAME	IN/OUT	FUNCTION
1	DBUS 0	I/O.	Memory data bus (LSB)
2	ADD 1	O	Address bus to VSM (LSB)
3	ROMCLK	O	Clock to VSM
4	VDD	I	Drain supply voltage (-5 V NOM)
5	Vss	I	Substrate supply voltage(+5 V NOM)
6	OSC	I	Oscillator input
7	T11	O	Sync
8	SPEAKER	O	Audio Output
9	I/O	O	Serial data out
10	PROM OUT	O	Testing use only
11	Vref	I	Ground reference voltage.
12	DBUS 5	I/O	Memory Data Bus
13	DBUS 6	I/O	Memory Data Bus
14	DBUS 7	I/O	Memory Data bus (MSB)
15	M0	O	Command bit 0 to VSM
16	M1	O	Command bit 1 to VSM
17	INT	O	Interrupt (active low)
18	READY	O	Transfer cycle W/CPU complete(active low)
19	DBUS 4	I/O	Memory data bus
20	TEST	I	Testing use only(do not connect)
21	ADD8/DATA	I/O	Address to VSM and serial data in MSB
22	DBUS 3	I/O	Memory data bus
23	ADD 4	O	Address bus to VSM
24	DBUS 2	I/O	Memory data bus
25	ADD 2	O	Address bus to VSM
26	DBUS 1	I/O	Memory data bus
27	WS	I	Write select (active low)
28	RS	I	Read select (active low)

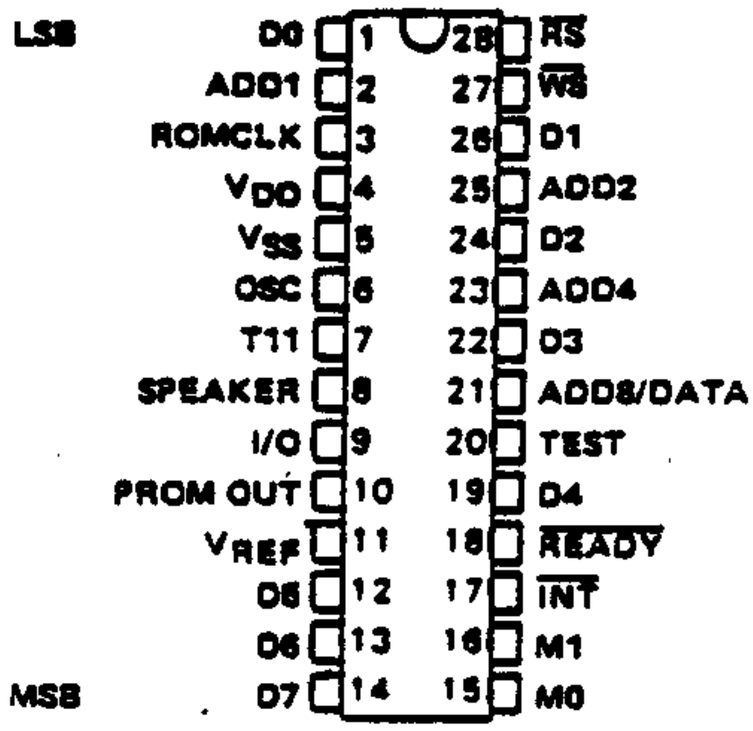


FIGURE 2-1. PIN ASSIGNMENTS AND LOCATIONS

2.2 I/O STRUCTURE

The VSP has two input holding registers, a Command Register, and a 128-bit FIFO Buffer. It also contains two output holding registers, the Data Register, and the Status Register. Transfer of data occurs along an eight-bit data bus that incorporates internal pull-up resistors and latched inputs.

During a Write cycle from the CPU, the control logic of the VSP routes data from the Memory Data Bus to either the FIFO Buffer, if a Speak External Command is executing, or, in all other cases, the Command Register. Once this data has been latched, the VSP signals completion of the data transfer to the CPU by lowering the READY Line to its active (low) condition. Similarly, on a Read cycle, when RS goes active (low), the VSP puts either the contents of the Data Register on the bus (if the preceding command was a Read Byte command) or the contents of the Status Register (all other cases). Following is a block diagram of the VSP and a more detailed discussion of the I/O structure.

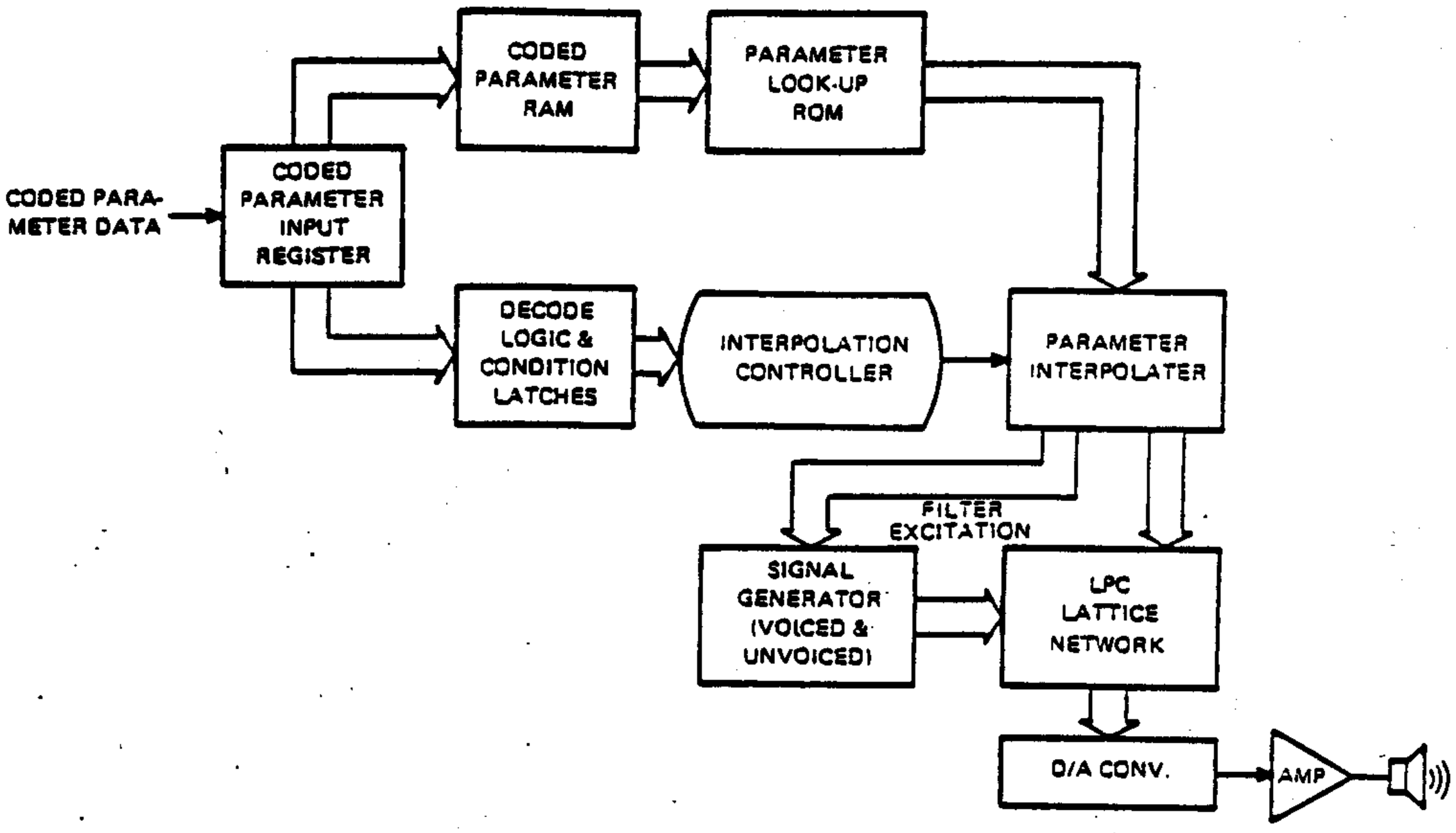


FIGURE 2-2. TMS5220C Processor Block Diagram

2.2.1 Command Register

The Command Register receives command data from the Memory Data Bus and holds it for the Controller to interpret and execute. The VSP behaves as an attached processor to the host CPU and performs its synthesis tasks when appropriate commands are sent by the host CPU. Details of the individual commands are found in section 2.3.

2.2.2 FIFO Buffer

The 128-Bit FIFO Buffer is organized as a 16-byte parallel-in, serial-out buffer. This buffer is used to hold speech data passed from the CPU to be processed by a Speak External command in the VSP. As required by the synthesis section, data is shifted out serially starting with the "First-in" byte. A Stack Pointer keeps track of the location of the "Last-In" byte and data from the CPU is always loaded just above this location. When the stack becomes less than half full (i.e., eight byte locations are void of data), the buffer low status condition (BL) becomes true. This signals the CPU that more data should be provided to the VSP. If the buffer empties completely, the

buffer empty status (BE) becomes true and the Talk Status Latch is reset causing speech to terminate immediately. To resume speech with data provided by the CPU, another Speak External command must be issued. Please note that the FIFO is cleared at the beginning and termination of the Speak External command. In addition, the Reset command and the Power-Up Clear sequence will clear the FIFO buffer.

2.2.3 Data Register

The eight-bit Data register is organized as a serial-in, parallel-out holding register. This register is used by the VSP to formulate a byte of data from serial data fetched from the VSM during the execution of a Read Byte command. When the Data Register has been loaded and the RS goes active (low), the byte is transfered to the Memory Data Bus. Note, the MSB is D7. Finally, the $\overline{\text{READY}}$ line goes low when the data is stable. (See Figure 2-2.)

2.2.4 Status Register

The three bits of the Status Register provide up-to-date information to the CPU on the state of the VSP. The Status Register may be read at any time except immediately following a Read Byte command. When RS goes active (low) the VSP routes the status data to the Memory Data Bus and lowers the Ready Line when the data is stable. Following is a description of the three status register bits along with their corresponding memory data bus bit.

MEMORY DATA BUS BIT	STATUS REGISTER BIT	DESCRIPTION
D7	TS	Talk Status is active (high) when the VSP is processing speech data. Talk Status goes active at the initiation of a Speak command or after nine bytes of data are loaded into the FIFO following a Speak External command. It goes inactive (low) when the stop code (Energy = 1111) is processed, or immediately by a buffer empty condition, or by a Reset command. The audio output is interpolating to zero during this frame and is terminated on the next frame boundry.
D6	BL	Buffer Low is active when the FIFO Buffer is more than half empty. Buffer Low is set when the "Last-In" byte is shifted down past the half-full boundary (becomes the eighth data byte) of the stack. Buffer Low is cleared when data is loaded to the stack so that the "Last-In" byte lies above the half-full boundary

and becomes the ninth data byte of the stack.

D5 BE

Buffer Empty is active (high) when the FIFO buffer has run out of data while executing a Speak External command. Buffer Empty is set when the last bit of the "Last-in" byte is shifted out to the synthesis section. This causes Talk Status to be cleared. Speech is terminated at some abnormal point and the Speak External command execution is terminated. Data from the Memory Data Bus is once again routed to the Command Register.

2.2.5 Analog Audio Out

The output of the D/A converter is a current source designed to deliver 0 to 1.5 milliamperes with resolution to 5.9 microamperes. Given a 1.8-kilohm load, the VSP will deliver between 0 and 2.7 volts. See Section 3. system interface for further details on interface.

2.3 COMMANDS

The CPU has minimal control over the VSP. Primarily the CPU passes commands to the VSP which initiates the activity. When WS becomes active (low), assuming a Speak External command is not presently executing, the data on the memory data bus is latched into the command register. Once the transfer is complete the VSP activates READY (low) to release the CPU. Next, the VSP interprets and executes the command. If the user tries to pass a command to the VSP while another command is executing the new command will not be accepted until the previous command is finished. The VSP will instruct the CPU to initiate wait states until it presents a READY flag to tell the CPU the present command has been fully executed. The commands available for use by the CPU and the command execution for each instruction are shown in Table 2-2 and described in the following sub sections.

TABLE 2-2. VSP COMMANDS AND COMMAND FORMAT

DATA BUS COMMAND CODE (D7-D0) (D7=MSB D0=LSB)	OPERATION
76543210	
X100AAAA	LOAD ADDRESS
X101XXXX	SPEAK
X110XXXX	SPEAK EXTERNAL
X001XXXX	READ BYTE
X011XXXX	READ AND BRANCH
XOXOX8CC	LOAD FRAME RATE
X111XXXX	RESET

A = Address
B = Variable frame rate option
X = Don't care
CC = Command Code bits

2.3.1 Load Address

The Load Address command allows the CPU to alter the address register of the VSM to point to new speech data. Each Load Address command modifies 4 bits (one nibble) of the VSM address register starting with the least significant nibble. An internal address pointer automatically controls the loading of all address nibbles and is reset when a Read Byte, Read and Branch, or a Speak command is executed.

Figure 2-3 demonstrates the use of the Load Address command required to address TMS6100 family speech memories. Five consecutive Load Address commands are required to load a 4 bit chip select address (selects one of 16 TMS6100 memory devices) and a 14 bit byte address (selects one byte within the selected 6100). The chip select address is mask-programmed during the manufacture of the memory device. Preprogrammed-off the shelf memory devices generally have a chip select address = 0000.

D7	D6	D5	D4	D3	D2	D1	D0	
X	1	0	0	A3	A2	A1	A0	First byte sent to VSP
X	1	0	0	A7	A6	A5	A4	
X	1	0	0	A11	A10	A9	A8	
X	1	0	0	CS1	CS0	A13	A12	
X	1	0	0	X	X	CS3	CS2	Last byte sent to VSP

(Load address command)

Note:
A0 = LSB of byte address
CS0 = LSB of chip select address
X = Don't care

FIGURE 2-3. LOAD ADDRESS SEQUENCE

2.3.2 Speak

The Speak command allows speech data to be generated from phrase data stored in the VSM. This command generates an internal signal that immediately causes Talk Status to be set and initiates speech synthesis calculations using the next available data from the VSM. Audio output begins on the following frame boundary. The VSP continues to fetch data from the VSM and generates speech output until a stop code (energy = 1111) is received and recognized. At such time the audio output begins to interpolate down to the zero energy level. On the next frame boundary, speech has ended, the Talk Status is cleared, and execution of the Speak command is completed. This activity is shown in Figure 2-5.

The Reset command will cause immediate termination of the Speak command and clear talk status. Audio output will halt immediately without waiting for a frame boundary.

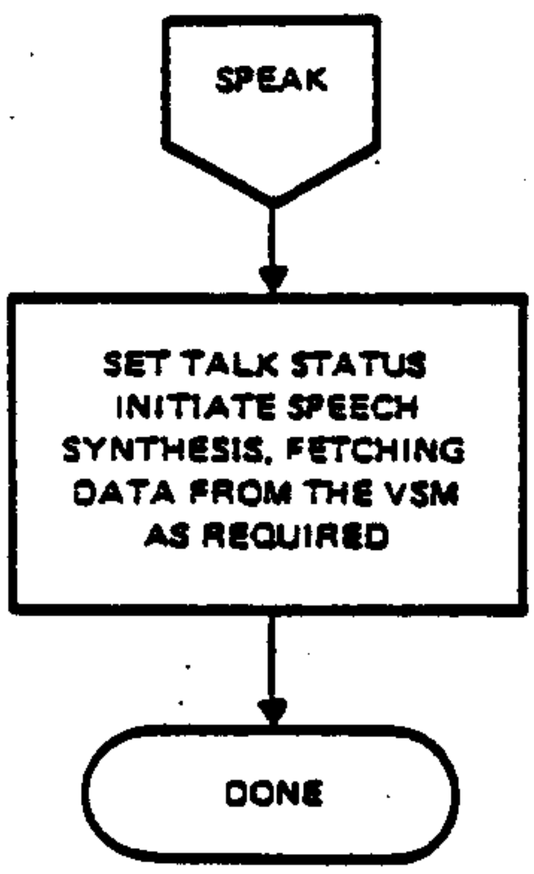


FIGURE 2-4. SPEAK COMMAND

2.3.3 Speak External

The Speak External command allows the CPU to supply speech data to the VSP from some memory other than the VSM. Upon receipt of a Speak External command, the VSP purges the FIFO buffer. At this time BL and BE become active (high) an interrupt is generated, and directs data written into the VSP to the FIFO. The VSP idles waiting for the CPU to fill the buffer before speech begins. When the buffer low status becomes false, by the CPU loading a minimum of nine bytes to the FIFO, Talk Status is set and speech synthesis calculations begin using data from the FIFO. Data continues to be taken from the FIFO until a Stop(energy = 1111) or the buffer empty abnormal termination occurs. While the Speak External command is executing, all data written to the VSP is routed to the FIFO buffer. All data transfered to the VSP after executing a Speak External command goes into the FIFO until a stop code read by the VSP, buffer empty, abnormal termination or hardware clear occurs (WS RS low). Refer to the following flow chart for further explaination.

2.3.4 Read Byte

The Read Byte command allows the CPU to access the next eight bits from the VSM (ignoring byte boundries). In order to access data or text at a particular address in any VSM, the full address is first loaded into the VSM address register using load address commands. Refer to the TMS6100 Data Manual.

2.3.5 Read and Branch

The Read and Branch command allows the VSP to access speech data via an indirect addressing scheme. This feature is typically used in conjunction with a look-up table stored in the initial address space of the VSM. The look-up table contains the actual addresses for the phrases stored in the ROM. Each look-up table entry occupies two bytes.

The advantage of this approach lies in the use of standardized software and hardware for different applications. One example might be the use of several languages in a common control system. Each language would be stored in the same place in the look-up table contained in each VSM.

To perform the Read and Branch operation the look-up table address is first loaded into the VSM address register with "Load Address" commands. Execution of the Read and Branch command ends with the VSM ready to speak starting at the address pointed to by the address contained in the look-up table. (See Figure 2-2) This command can not be used in multiple VSM applications.

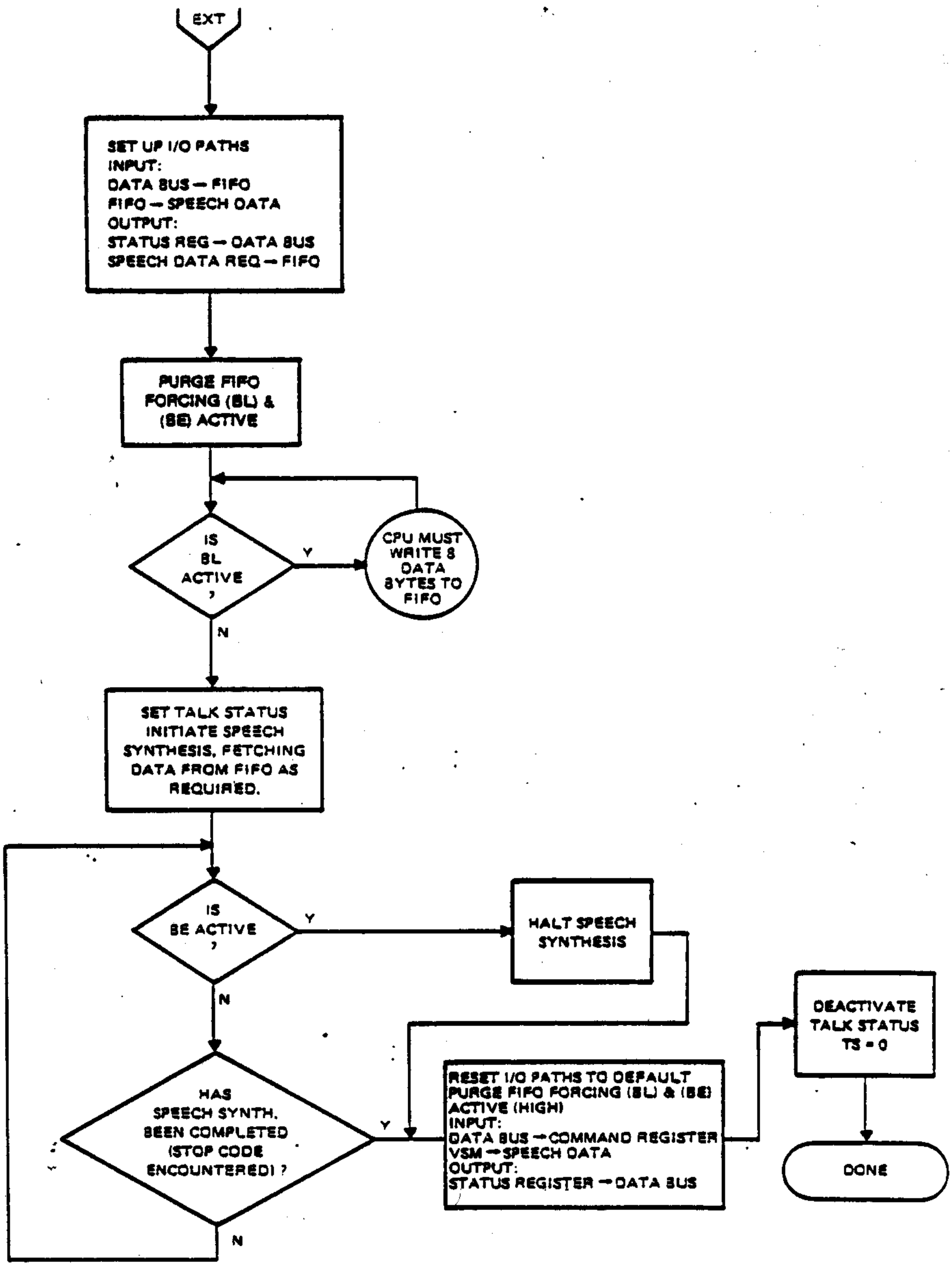


FIGURE 2-5. SPEAK EXTERNAL COMMAND

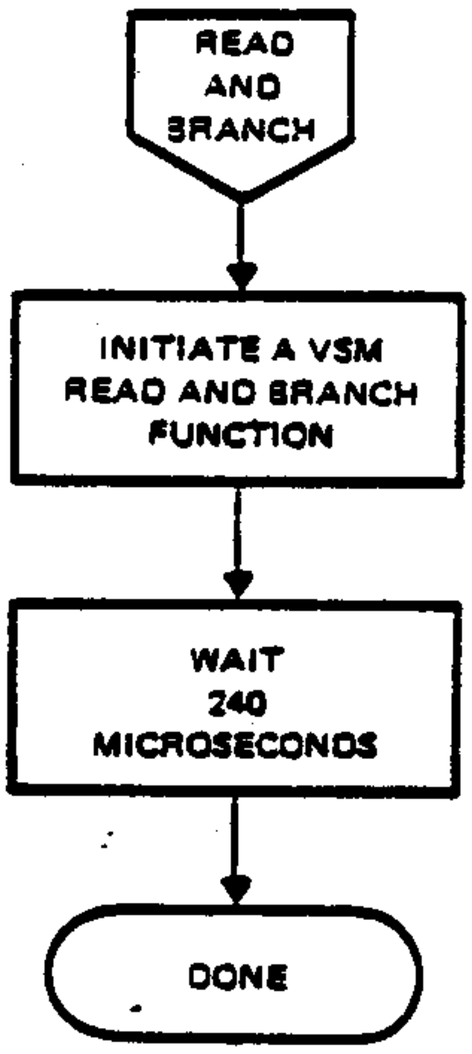


FIGURE 2-6. READ AND BRANCH

2.3.6 Load Frame Rate

This unique feature of the TMS5220C provides a range of data-rate/speech- quality trade offs. A frame rate of 200 samples/frame is most generally used and is the default rate selected by the Hardware Clear sequence at power up. If a rate of 200 samples/frame is to be used then the Load Frame Rate command is not required.

Two methods are provided for specifying other frame rates. The selectable method (D2=0) directly specifies the desired frame rate using two control bits within the Load Frame Rate Command (see Table 2-3). The variable method (D5=1) allows the rate information included with the data to determine the correct frame rate. This mode is entered by executing the Load Frame Rate command with bit D2 = 1 (2 control bits required). Refer to Table 2-4 for control bit coding and see Figure 2-4.

TABLE 2-3. - FRAME RATE CONTROL BITS -- NON - DATA STREAM DEPENDENT

D7	D6	D5	D4	D3	D2 E	D1 C	D0 C	FRAME RATE SAMPLES/FRAME
X	0	X	0	X	0	0	0	200
X	0	X	0	X	0	0	1	150
X	0	X	0	X	0	1	0	100
X	0	X	0	X	0	1	1	50

TABLE 2-4. - SELECTABLE FRAME OPTIONS -- DATA STREAM DEPENDENT

MSB	LSB	FRAME RATE SAMPLES/FRAME
0	0	200
0	1	150
1	0	100
1	1	50

2.3.7 Reset

The Reset command allows the CPU to halt the Speak command and to put the VSP into a known state. Reset clears the Talk status, halting speech activity immediatly. The 128-bit FIFO Buffer is purged (BL and BE become active[high]) and the I/O paths are set to their default condition. In addition, the interupt line (INT) becomes inactive (high). Also note, the Reset command cannot halt the Speak External command because the Reset command is recognized as speech data. WS and RS low at the same time is the ultimate form of reset. To achieve a known state, set WS and RS low followed by a Reset Command.

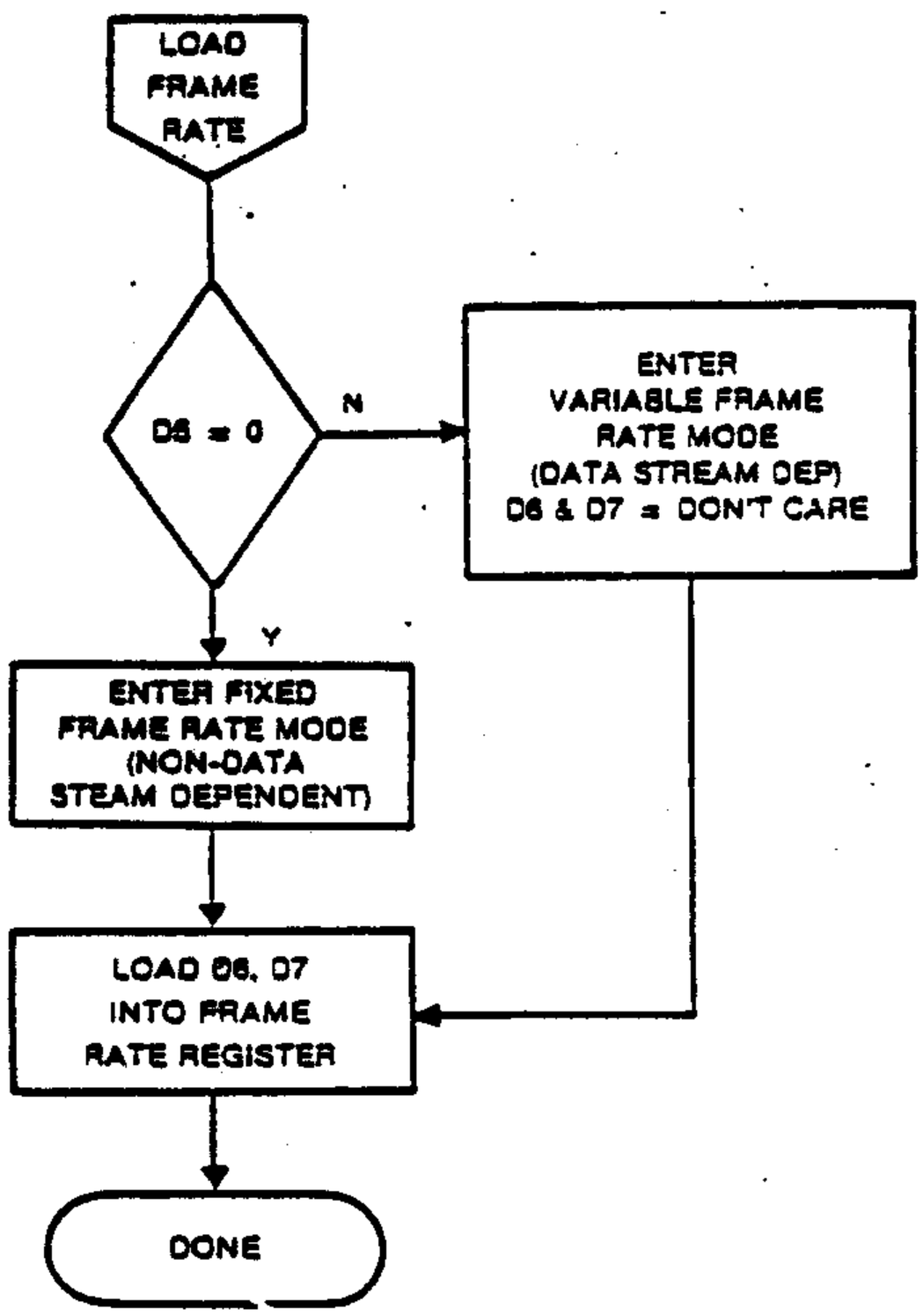


FIGURE 2-7. LOAD FRAME RATE

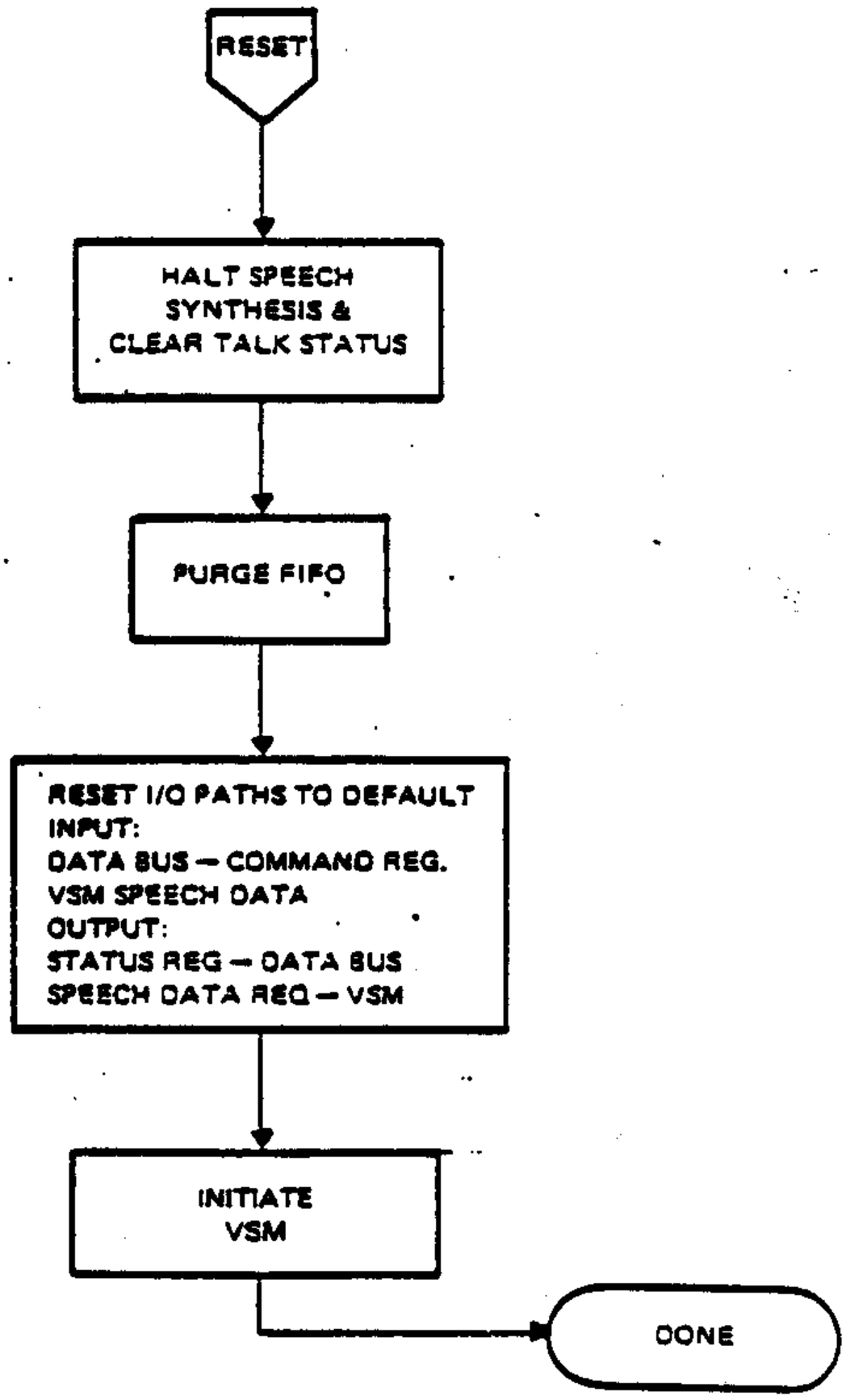


FIGURE 2-8. RESET COMMAND

2.4 TIMING

This section contains the system timing information. This includes a comparison of the system times at 10kHz and 8kHz (TABLE 2-5), a system timing summary, and individual timing diagrams for commands and status transfers.

SAMPLE RATE	10kHz	8kHz
FRAME RATE		
200 SAM./FR	50. Hz	40 Frame/sec
150 SAM./FR	66.7 Hz	53.3 Frame/sec
100 SAM./FR	100. Hz	80 Frame/sec
50 SAM./FR	200. Hz	160 Frame/sec
FRAME PERIOD		
200 SAM./FR	20 ms	25 ms
150 SAM./FR	15 ms	18.75 ms
100 SAM./FR	10 ms	12.5 ms
50 SAM./FR	5 ms	6.25 ms
INTERPOLATION RATE	400 Hz	320 Hz
INTERPOLATION INTERVAL	2.5 ms	3.125 ms
NUMBER OF INTERPOLATIONS		
200	8	8
150	6	6
100	4	4
50	2	2
SAMPLE RATE	10 kHz	8 kHz
SAMPLE PERIOD	100 us	125 us
ROM CLOCK RATE	200 kHz	160 kHz
ROM CLOCK PERIOD	5 us	6.25 us
RC OSC RATE	800 kHz	640 kHz
RC OCS PERIOD	1250 ns	1562.5 ns

NOTE: All timing references in this data manual are based on an 8-kHz sample rate.

2.4.1 Write Cycle for Read and Branch, Load Address, Speak, Speak External, and Reset Commands

timing requirements

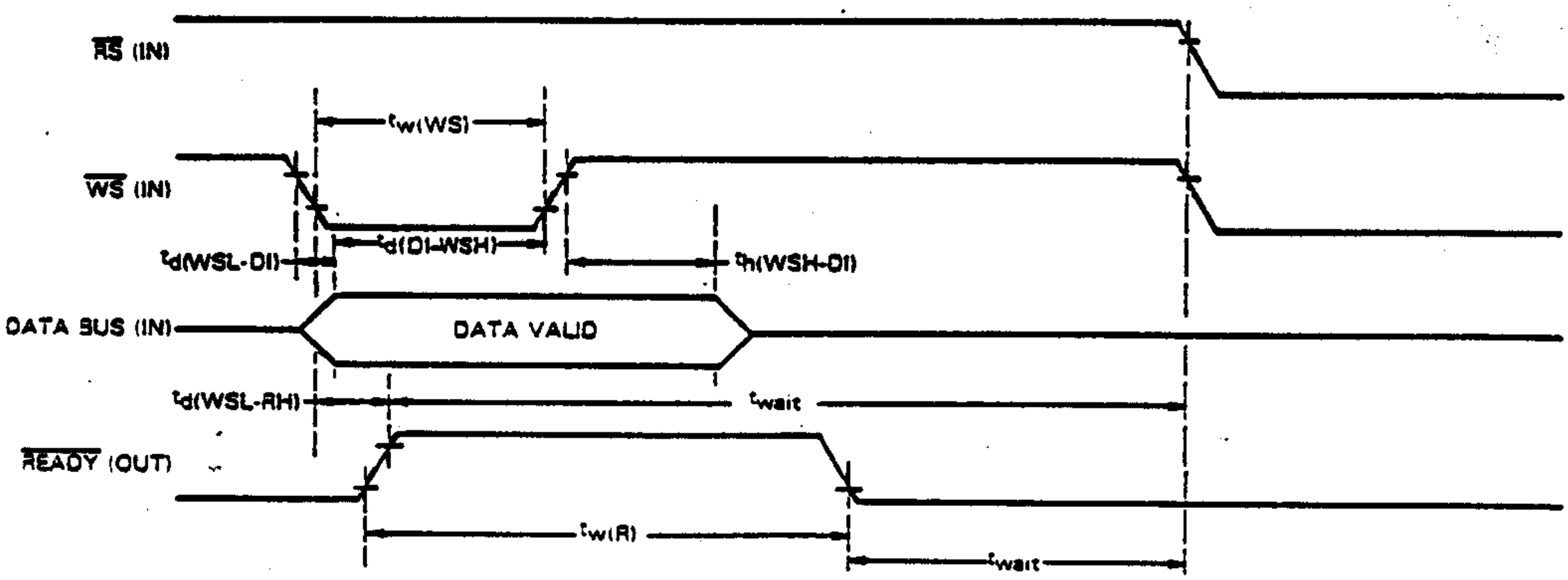
PARAMETER		MIN	NOM	MAX	UNIT
$t_{d(WSL-DI)}$	Delay time from $\overline{WS}$ low to data valid			3	μs
$t_{d(DI-WSH)}$	Delay time from data in valid to $\overline{WS}$ high	200			ns
$t_{h(WSH-DI)}$	Data hold time	100			ns
$t_{w(WS)}$	$\overline{WS}$ low time	200			ns
t_{wait}	Read-and-branch command wait time from $\overline{READY}$ high until next allowable* command	595			μs
t_{wait}	Load address command wait time from $\overline{READY}$ high until next allowable* command	42			μs
t_{wait}	Speak command wait time from $\overline{READY}$ high until next allowable* command — Preceded by load-address command	287			μs
	Speak command wait time from $\overline{READY}$ high until next allowable* command — Not preceded by load-address command	56			μs
t_{wait}	Speak external command wait time from $\overline{READY}$ high until next allowable* command	42			μs
t_{wait}	Reset command wait time from $\overline{READY}$ high until next allowable* command	300			μs

switching characteristics

PARAMETER		MIN	NOM	MAX	UNIT
$t_{d(WSL-RH)}$	Delay time from $\overline{WS}$ low to $\overline{READY}$ high			100	ns
$t_{w(R)}$	$\overline{READY}$ high pulse width	18		26	μs

All timing is based on a clock frequency of 8 kHz.

* If a new command is issued prior to the completion of the present command (before the end of t_{wait}), then the $\overline{READY}$ signal will go high and stay high until the present command is finished executing in the VSP.



2.4.2 Write Cycle for Speak External Speech Data

timing requirements

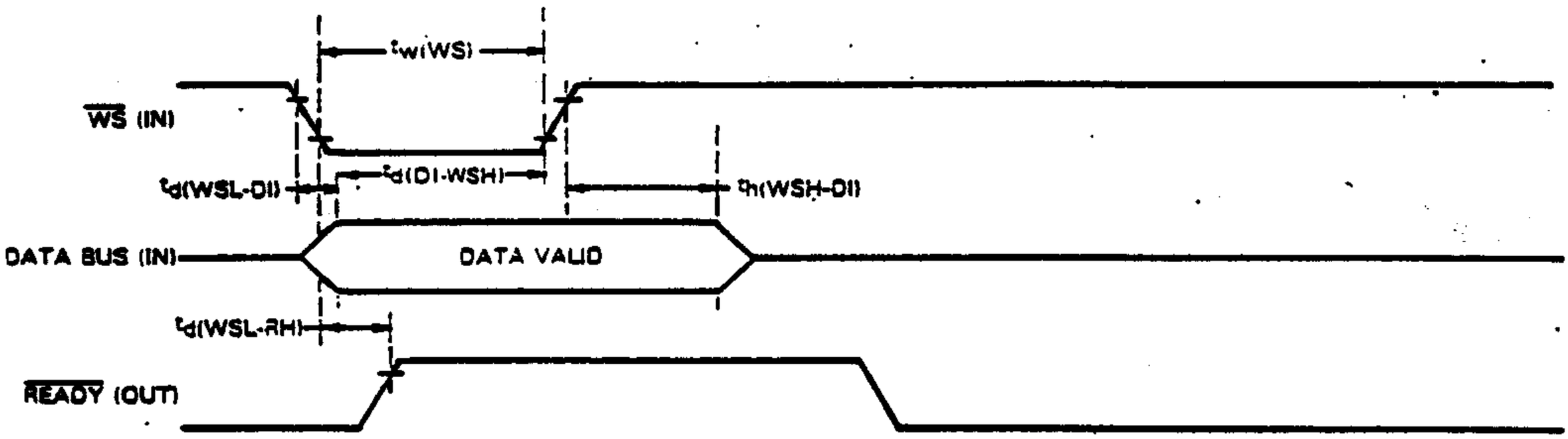
	PARAMETER	MIN	NOM	MAX	UNIT
$t_{d(WSL-DI)}$	Delay time from $\overline{WS}$ low to data valid			3	μs
$t_{d(DI-WSH)}$	Delay time from data in valid to $\overline{WS}$ high	200			ns
$t_{h(WSH-DI)}$	Data hold time	100			ns
$t_{w(WS)}$	$\overline{WS}$ low time	200			ns
t_{wait}	Wait time from $\overline{WS}$ high until next allowable access	10			μs

switching characteristics

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{d(WSL-RH)}$	Delay time from $\overline{WS}$ low to $\overline{READY}$ low			100	ns
$t_{w(R)}$	$\overline{READY}$ high pulse width	18		26	μs

All timing is based on a clock frequency of 8 kHz.

* If a new command is issued to the VSP prior to the completion of the present command then the $\overline{READY}$ signal will go high and remain high until the completion of the present command as defined by t_{wait} above.



2.4.3 Read Cycle for Status Transfers

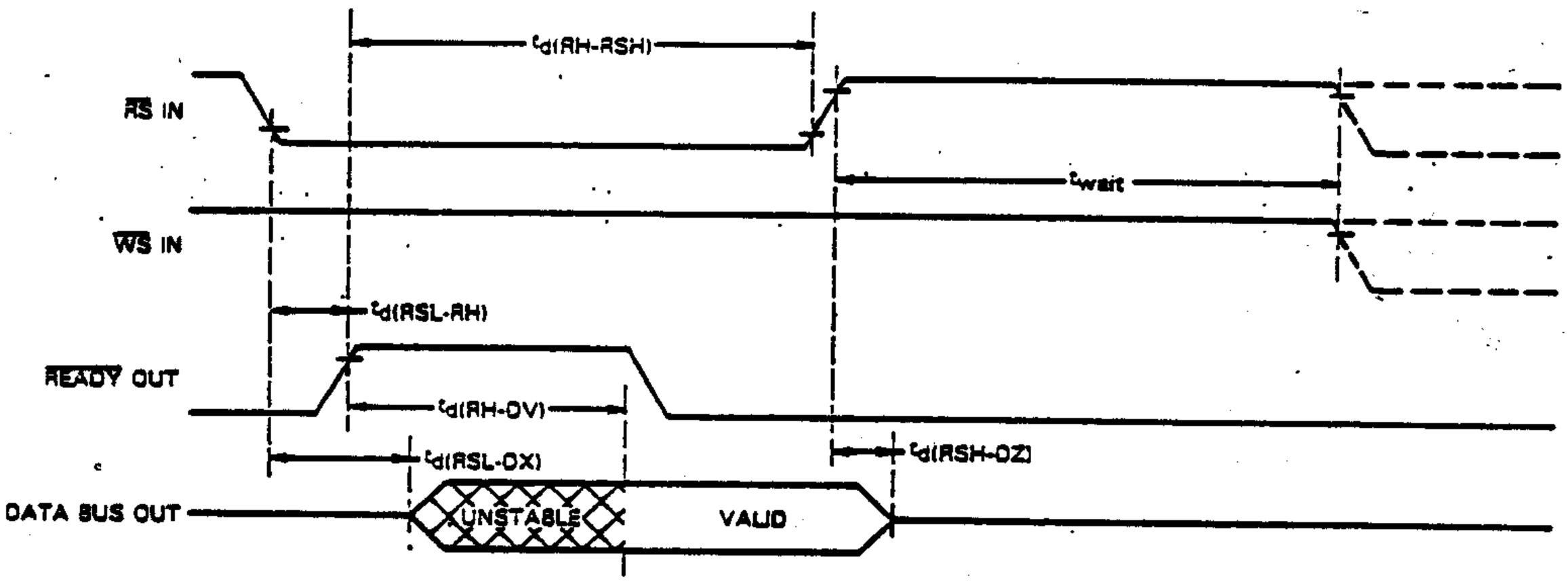
timing requirements

	PARAMETER	MIN	NOM	MAX	UNIT
$t_{d(RH-RSH)}$	Delay time from $\overline{READY}$ high to $\overline{RS}$ high	6			μs
t_{wait}	Wait time from $\overline{RS}$ high to next allowable* command	12			μs

switching characteristics

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{d(RSL-RH)}$	Delay time from $\overline{RS}$ low to $\overline{READY}$ high			100	ns
$t_{d(RH-DV)}$	Delay time from $\overline{READY}$ high to data valid (stable)	6		11	μs
$t_{d(RSL-DX)}$	Delay time from $\overline{RS}$ low to data bus driven (output unstable)		$t_{d(RH-DV)} - 2$		μs
$t_{d(RSH-DZ)}$	Delay time from $\overline{RS}$ high to data output disabled		Z	10.5	μs

* If a new command is issued to the VSP prior to the completion of the present command, then after the $\overline{READY}$ signal goes high, in its normal response time, it will remain high until the present command has been fully executed by the VSP.



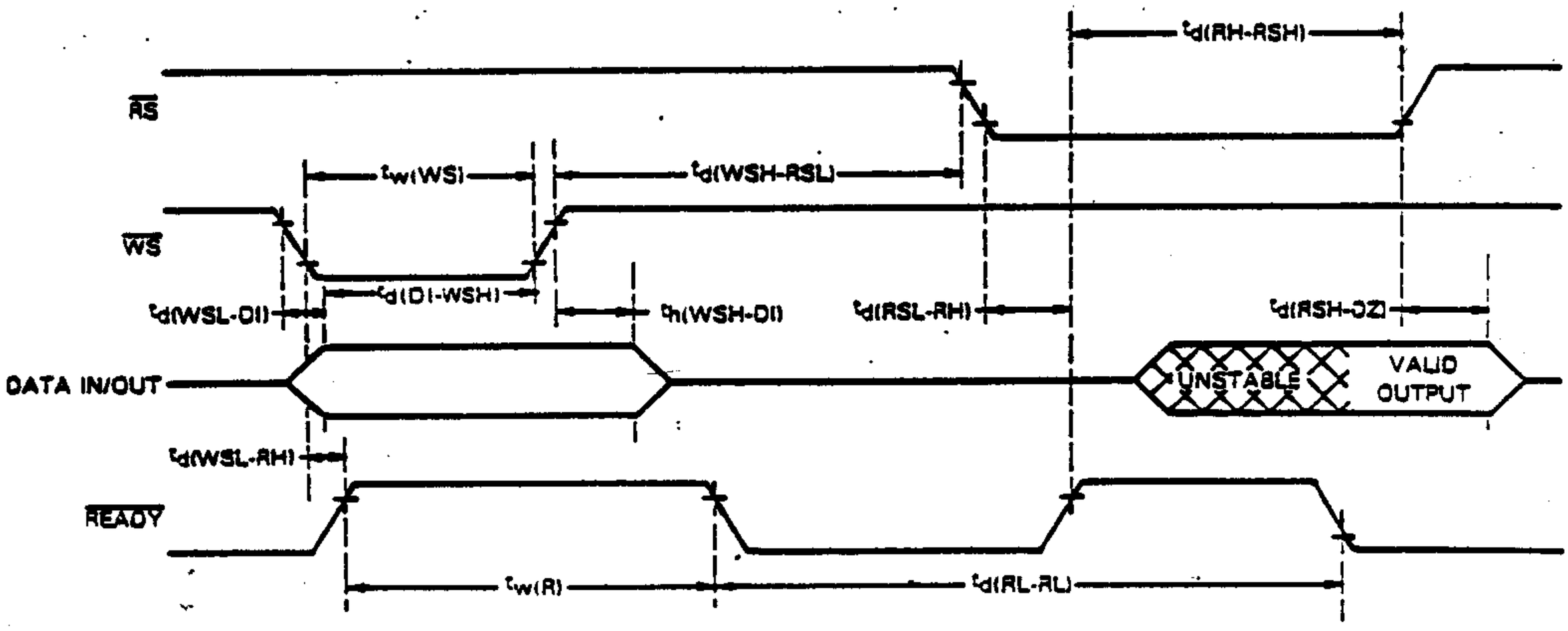
2.4.4 Read Byte Sequence

timing requirements

	PARAMETER	MIN	NOM	MAX	UNIT
$t_{d(WSL-DI)}$	Delay time from $\overline{WS}$ low to data valid			3	µs
$t_{d(DI-WSH)}$	Delay time from data in valid to $\overline{WS}$ high	200			ns
$t_{h(WSH-DI)}$	Hold time of data in after $\overline{WS}$ high	100			ns
$t_{d(RH-RSH)}$	Delay time from $\overline{READY}$ high to $\overline{RS}$ high	8			µs
$t_{d(WSH-RSL)}$	Delay time from $\overline{WS}$ high to $\overline{RS}$ low	12			µs
$t_{w(WS)}$	$\overline{WS}$ low time	200			ns

switching characteristics

	PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(WSL-RH)}$	Delay time from $\overline{WS}$ low to $\overline{READY}$ high				100	ns
$t_{d(RSL-RH)}$	Delay time from $\overline{RS}$ low to $\overline{READY}$ high				100	ns
$t_{w(R)}$	$\overline{READY}$ high pulse width (write)				26	µs
$t_{d(RL-RL)}$	Delay time from $\overline{READY}$ low (write) to $\overline{READY}$ low (read)	No previous load address			320	µs
		Previous load address			440	
$t_{d(RSH-DZ)}$	Delay time from $\overline{RS}$ high to data output disabled		4		3	µs



SECTION 3

SYSTEM INTERFACE

3.1 SYSTEM CLOCK

As previously mentioned, this manual describes all VSP timing at an 8-kHz sample rate. This requires that the system clock run at 640 kHz. Variations from this rate will cause the pitch of the speech to vary. The 640kHz corresponds to a ROM clock rate of 160kHz. This signal is buffered and not affected by measurement instrument capacities.

The RC oscillator may be adjusted to correspond to the sampling frequency used when orginally encoding the speech. Use of a shunt capacitor is recommended to prevent circuit layout and environmental stray noise from affecting device operation. A trimmer potentiometer is required because frequency varies part to part and depending on the operating voltage. See Figure 3-1a

Additionally the OSC pin can be driven directly with a 320kHz squarewave clock if the PROMOUT pin is held at Vss potential. The clock input must be a 0 to 5 volt signal. If PROMOUT is left open or held at Vref or Vdd level, the internal RC oscillator is active. To set the RC oscillator frequency, connect a frequency counter to the ROM clock output of the TMS5220C and trim the reading to 160kHz for 8kHz sampled data or to 200kHz for 10kHz sampled data. See Figure 3-1B.

A mask-programmed option exists on the TMS5220C to allow use of a ceramic resonator instead of the RC oscillator. This option is specified during the manufacture of the TMS5220C and is therefore not user switchable. With this option, a 320 kHz squarewave clock input can still be used by connecting the promout pin to Vss (+5 volts). A 320 kHz ceramic resonator is required to provide an 8 kHz sample rate. A 400 kHz ceramic resonnator is required for a 10 kHz sample rate. See Figure 3-1C.

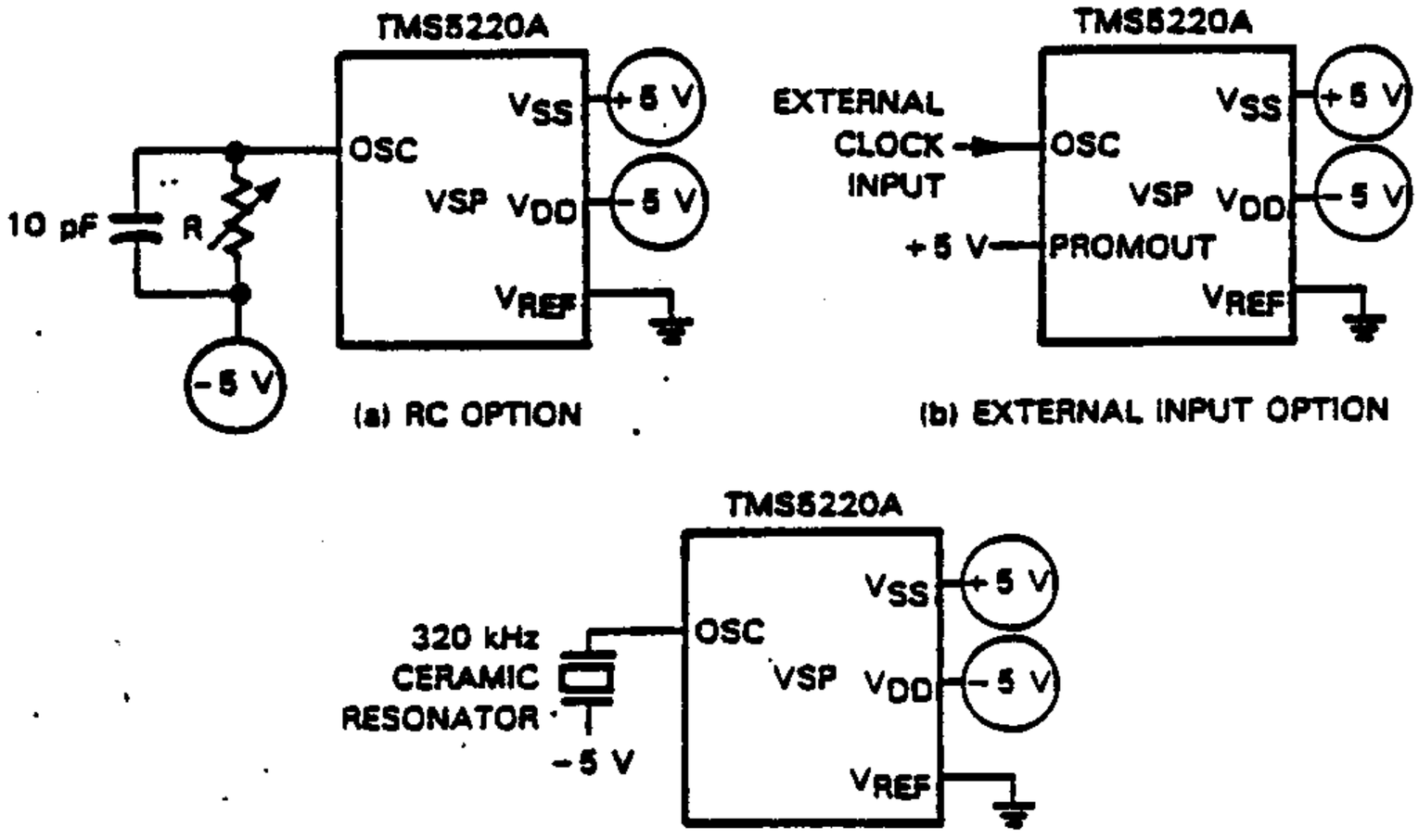


FIGURE 3-1. SYSTEM CLOCK

3.2 CPU INTERFACE

The CPU interface consists of an eight-bit bidirectional data bus (D7-D0), seperate selects for read operations and write operations, a ready line for synchronization and an interrupt line to indicate a status change on the VSP that requires CPU attention.

3.2.1 Read Select ($\overline{RS}$) and Write Select ($\overline{WS}$)

VSP activity on the memory data bus is controlled by the Read Select ($\overline{RS}$) and the Write Select ($\overline{WS}$) lines as shown in Table 3-1. This activity is further demonstrated in Figure 3-2.

TABLE 3-1. RS AND WS FUNCTION

$\overline{RS}$	$\overline{WS}$	BUFFER CONDITION
H	H	High impedence state
H	L	Input to VSP. Some other device must be driving the Bus (typically the CPU).
L	H	Output from the VSP. No other device should be driving the bus at this time
L	L	Hardware Power-up Clear

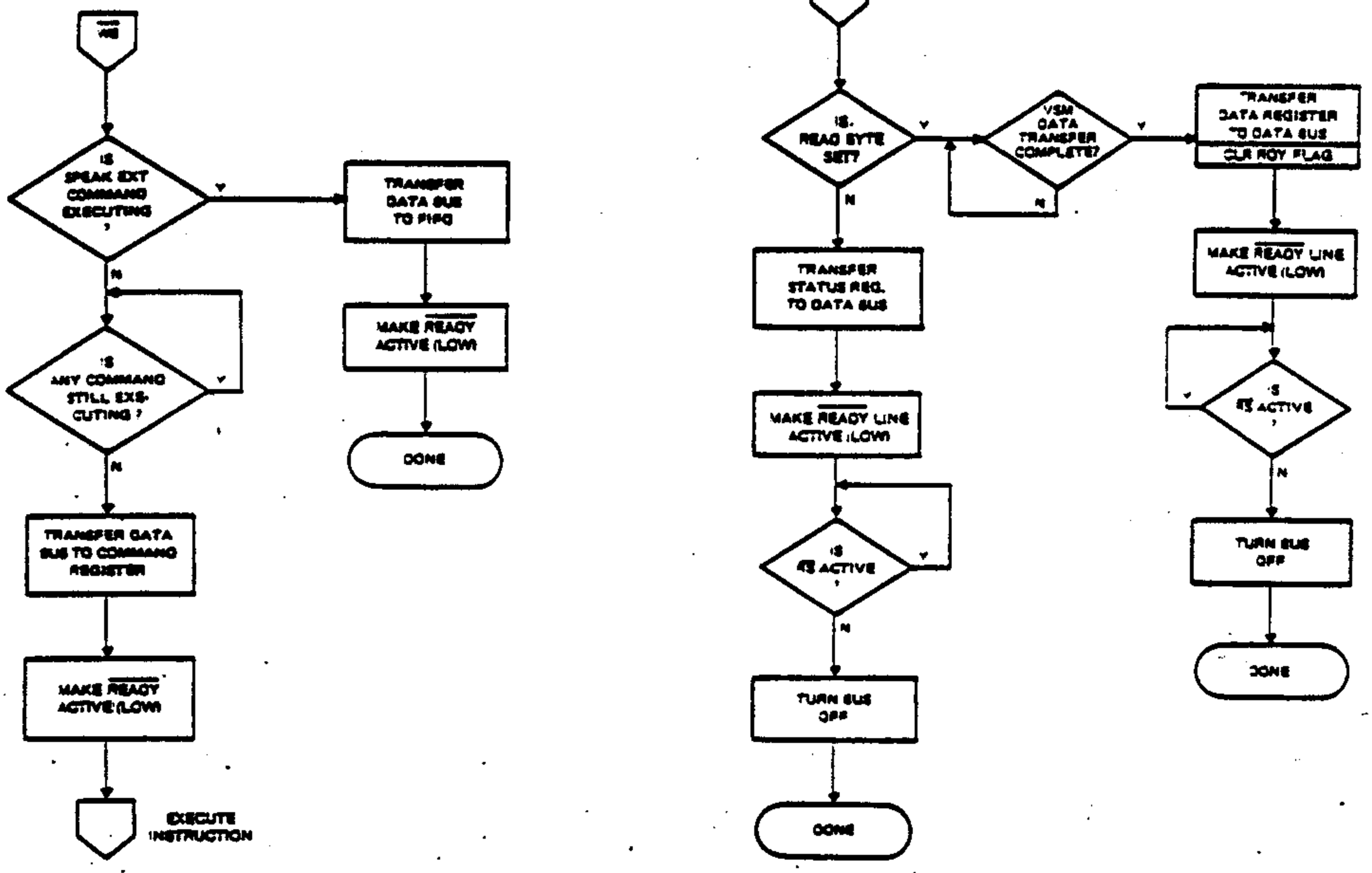


FIGURE 3-2. $\overline{WS}$ AND $\overline{RS}$ CONTROL OF MEMORY DATA BUS

It is important to note that no device can successfully complete a read cycle (from the VSP) while $\overline{WS}$ is active (low) nor can a successful write cycle (to the VSP) be carried out while $\overline{RS}$ is active (low). If $\overline{WS}$ and $\overline{RS}$ are low simultaneously, the device will initiate the power-up sequence.

3.2.2 Ready

The TMS5220C VSP is a slow memory device. This means that it cannot properly respond to system memory cycles within the minimum access time as determined by the CPU clock. Therefore the VSP requires wait states from the CPU to successfully complete a memory cycle. The effect of inserting wait states into memory access cycles is to extend the minimum allowable access time by one clock period for each wait state. The VSP controls the number of wait states executed by the CPU with the $\overline{READY}$ signal.

The $\overline{READY}$ line on the VSP will go high 100ns after $\overline{RS}$ or $\overline{WS}$ goes active (low) to let the CPU know that the data transfer cycle cannot yet be completed. When the VSP has established stable data on the data bus (in the case of $\overline{RS}$) or has completed latching data in from the

data bus (in the case of $\overline{WS}$), the READY line will go low indicating tnat the CPU may complete the data transfer cycle.

3.2.3 Interrupt

The interrupt line ($\overline{INT}$) indicates changes in the status of the VSP that may require CPU attention. INT goes inactive (high) when the Status Register is read or if the Reset Instruction is executed. $\overline{INT}$ goes active (low) under the following circumstances:

0 Talk Status (TS) makes a one-to-zero transition indicating the end of speech processing if TS makes a one-to-zero transition during a read cycle: tne interrupt will occur after tne read cycle has been completed.
0 Buffer Low (BL) makes a zero-to-one transition indicating that more phrase data needs to be supplied to the FIFO for Speak External command.

3.3 MEMORY INTERFACE

The VSP may receive data from tne CPU or directly access up to 16 VSM's. These VSM's can be tne TMS6100, tne TMS6125, or a custom speech ROM or EPROM developed for a specific application. Eproms may be used with added hardware or software.

Access to the VSM is accomplished with a four bit parallel bus (ADD 8, 4, 2, 1) two control lines (M0, M1), and a synchronizing clock (ROMCLK). For further information on the VSM consult the data manual for the ROM you are using.

Note that ADD8 is multiplexed as the Data Out line of the VSM as well as the most significant bit of the four bit address bus into the VSM.

3.4 HARDWARE CLEAR

After power has been applied, a hardware clear is performed by simultaneously setting $\overline{WS}$ and $\overline{RS}$ low for one milliesecond. The events caused by the Power-up Clear are similar to the Reset command as shown below.

0 Talk Status is cleared and any speech activity is halted.
0 The T State Counter is reset.
0 The FIFO is purged (BL &BE go active)
0 I/O multiplexers are set to allow data to be written to the Command Register and Status Register.
0 Frame period is set to 200 samples. Depending on the state of the device an interrupt may be generated.

SECTION 4

THEORY OF OPERATION

4.1 OVERVIEW OF LPC

Linear Predictive Coding (LPC) synthesizes human speech by recovering from the orginal speech enough data to construct a time-varying digital filter model of the vocal tract. This filter is excited with a digital representation of either glottal air impulses (voiced sound) or the rush of air, which produces unvoiced sounds. The output of this filter model is passed through an 8-bit digital-to- analog (D/A) converter to produce a synthetic speech waveform.

The LPC analysis program begins with a set of digitized speech samples. These digitized samples are usually derived with an analog-to-digital converter by sampling an analog waveform at a rate of 8 or 10 kHz. Consecutive samples are grouped together to form a "frame" of digitized samples. The frames may contain from 50 to 400 samples, but usually contain 200. The LPC analysis routine operates on these digitized samples, a frame at a time, by preemphasizing the samples, calculating the energy, pitch, and the spectral coefficients (K-parameters). Next, each value is coded according to a pre-selected coding table.

This coded speech parameter data is fed serially from either the VSM or the FIFO buffer to the parameter input register. Here the Controller unpacks the data and performs various tests (i.e., is the repeat bit set, is pitch zero, is energy zero). Once unpacked, the coded parameter data is stored in RAM to be used as the index value to select the appropriate value from the Parameter Look-Up ROM. The outputs of the Parameter Look-Up ROM are the target values for the interpolation logic to reach in this frame period. During each of the interpolation periods the interpolation logic sends new parameter values to the LPC lattice network which makes available a new value of digitized synthetic speech to the D/A converter.

4.2 CODED SPEECH PARAMETERS

The LPC method of speech encoding reduces the speech data rate from approximately 100,000 bits/sec (raw digitized speech) to about 4800 bits/sec. The analyzer reduces this rate further (to 2000 bits per second or less) by encoding each of the 10 bit speech parameters as 3 to 6 bit codes. These coded values select a 10-bit parameter from the parameter look-up ROM in the VSP. Depending on the influence of each parameter on speech quality, between 8 and 64 possible values are stored in the Look-Up ROM for decoding and use in synthesis calculations. Note that the parameter ROM in the TMS5220C is mask

programmable and not touchable or alterable by the user.

Table 4-1 summarizes the parameter coding for the TMS5220C.

TABLE 4-1. PARAMETER CODING

PARAMETER	LEVELS	CODE BITS
ENERGY	15	4
PITCH	64	6
K1	32	5
K2	32	5
K3	16	4
K4	16	4
K5	16	4
K6	16	4
K7	16	4
K8	8	3
K9	8	3
K10	8	3
12	127	49 + REPEAT = 50 BITS

Assuming an 8kHz sample rate, a full set of coded parameters for each frame would require a data rate of 40Hz X 50 bits or 2000 bits per second. There are, however, three special cases in which a full frame is not necessary which allows the average data for male speech to be reduced to approximatly 1200 bits per second. The first assumes that vocal tract shape changes occur slowly therefor making it possible to repeat previous reflection coefficient data. This repetition is facilitated with a contol bit added to each frame which follows the energy frame. This control bit is shown in Figure 4-1 as the repeat bit. For example, in a voiced frame if the repeat bit is 1 only energy and pitch data are accessed from the VSM and the previous K1-K10 values are retained. Secondly, unvoiced frames require fewer filter reflection coefficients. Consequently, when pitch = 000000(binary), only K1-K4 are fetched from the VSM and stored in the Parameter RAM. As shown in Figure 4-1, K5 - 10 are not required for for unvoiced frames. Finally, when energy = 0000 as in interword or intersyllable pauses, no other data is required.

The following figure shows the 10 possible data strings (imbeded frame frate control (52 bit) and data without frame control (50 bit)).

	Frame Rate Control Bits*	ENERGY		PITCH	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	
	xx	xxxx	x	xxxxxx	xxxxx	xxxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxx	xxx	xxx	
Voiced Frame (Variable Frame Rate)			0	52 Bits/	Frame										
Voiced Frame (Fixed Frame Rate)			0	50 Bits/	Frame										
Unvoiced Frame (Pitch = 0, Variable Frame Rate			0	000000											33 Bits/ Frame
Unvoiced Frame (Pitch = 0, Fixed Frame Pitch)			0												31 Bits/ Frame
Repeat Frame (Variable Frame Rate)			1												13 Bits/ Frame
Repeat Frame (Fixed Frame Rate)			1												11 Bits/ Frame
Zero Energy (Silence) (Variable Frame Rate)		0000													8 Bits/ Frame
Zero Energy (Silence) (Fixed Frame Rate)		0000													4 Bits/ Frame
Stop Code (Variable Frame Rate)		1111													8 Bits/ Frame
Stop Code (Fixed Frame Rate)		1111													4 Bits/ Frame

Not required for unvoiced frames

*These bits are only required when data dependent frame rate control has been selected.

FIGURE 4-1. FRAME DATA STRING LENGTHS

4.3 D/A CONVERSION

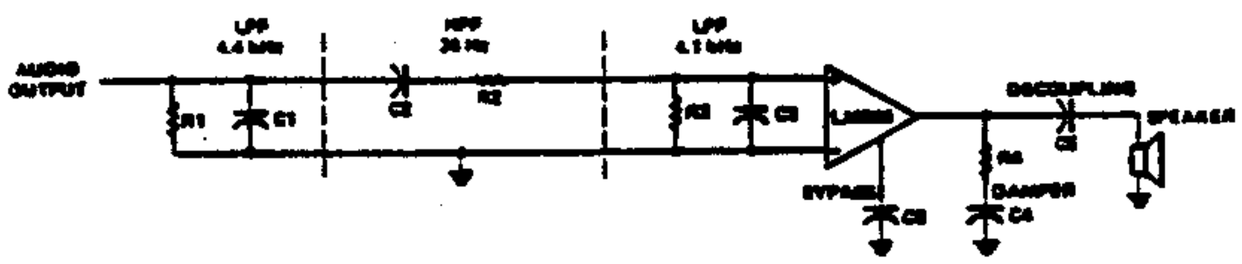
The TMS5220C contains an eight (8) bit digital to analog converter (D?A) with a typical linearity of one half of the least significant bit. Every smaple period (e.g. 125 microseconds) the lattice filter generates a new data point which is converted into a current output if zeri (0) to 1500 microamps. The output signal has as its most negative value, zero and as its most positive value, 1500 microamps. A resistor between the D/A output and ground is typically used as a current to voltage converter and a series capacitor is necessary to AC couple the speech output (the D/A has an offset binary output) to subsequent filter and amplifier stages. Figure 4-2 shows typical audio output circuits which may be used with the TMS5220C.

4.4 POWER UP SEQUENCE

In order to assure proper initialization of the TMS5220C during power up, the voltage rails (Vdd and Vss) must become stable within two (2) milliseconds. Figure 4-3 shows a timing diagram of the power up sequence. If the power up transition takes longer, then a hardware reset must be generated after the rails have stabilized. A hardware reset is performed by simultaneously driving RS and WS to their active (low) states. See Figure 4-3 for exact timing requirements.

4.5 DIGITAL AUDIO OUT

Digital speech prior to the internal digital to analog converter can be serially accessed from the TMS5220C. The speech is accessed as a signed 10-bit value on the I/O pin clocked by the ROMCLK output and synchronized by the T11 output. Figure 4-4 demonstrates how binary data can be accessed. CMOS buffers provide a TTL Interface to the PMOS 5220C.



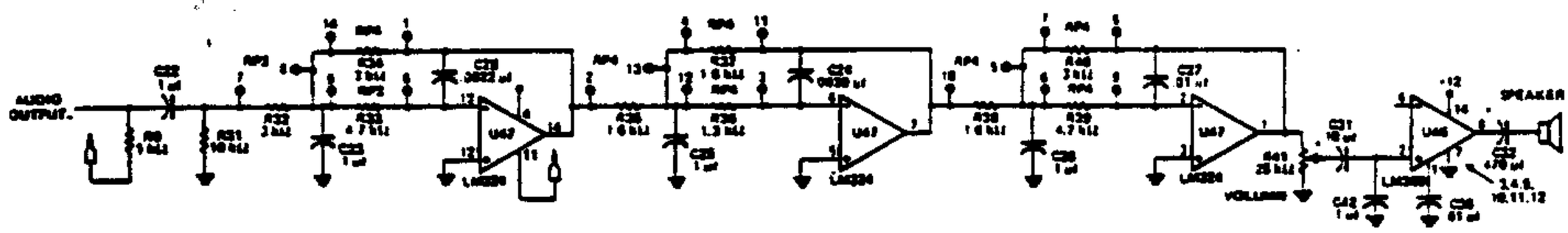


FIGURE 4-2. TYPICAL AUDIO OUTPUT CITCUITS FOR THE TMS5220C

PARAMETER	MIN	TYP	MAX	UNIT
t_{DSR}			2.0	µs
t_1	5.0			µs
t_2			50	ns
t_3	200			ns
t_4			50	ns

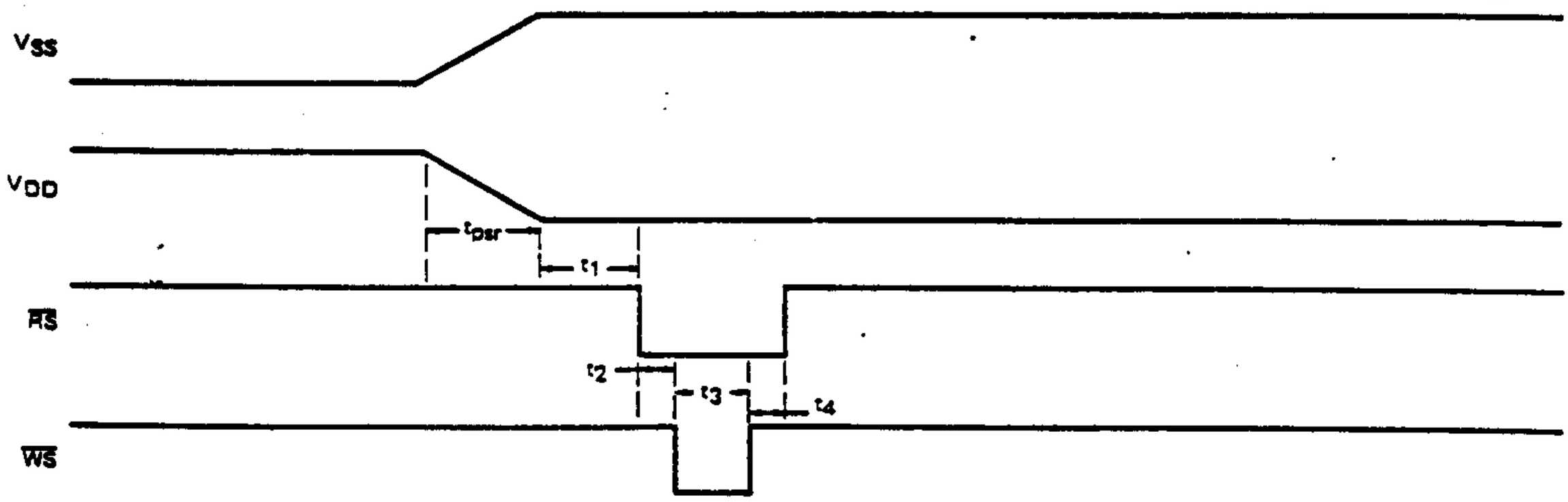
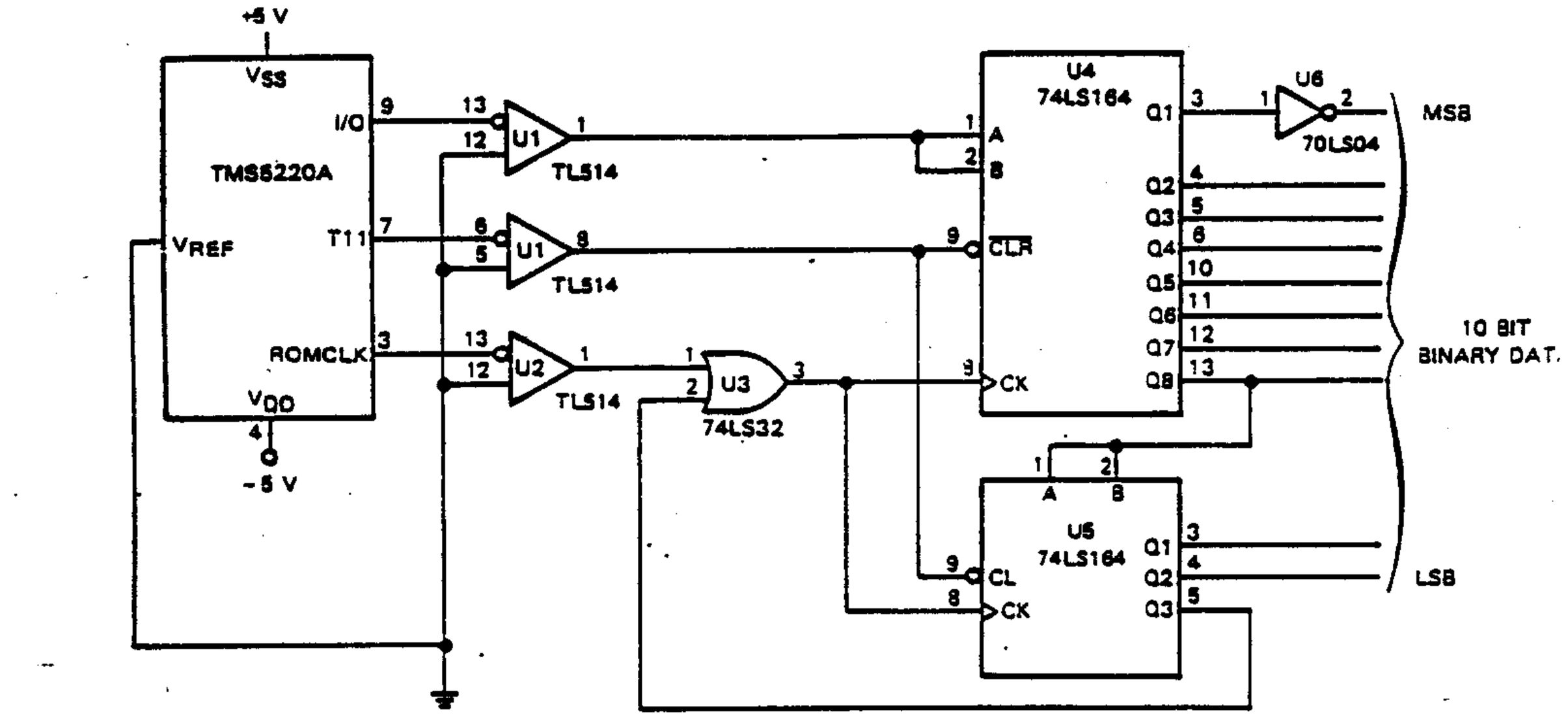


FIGURE 4-3. POWER UP SEQUENCE FOR THE 5220C SPEECH SYNTHESIZER



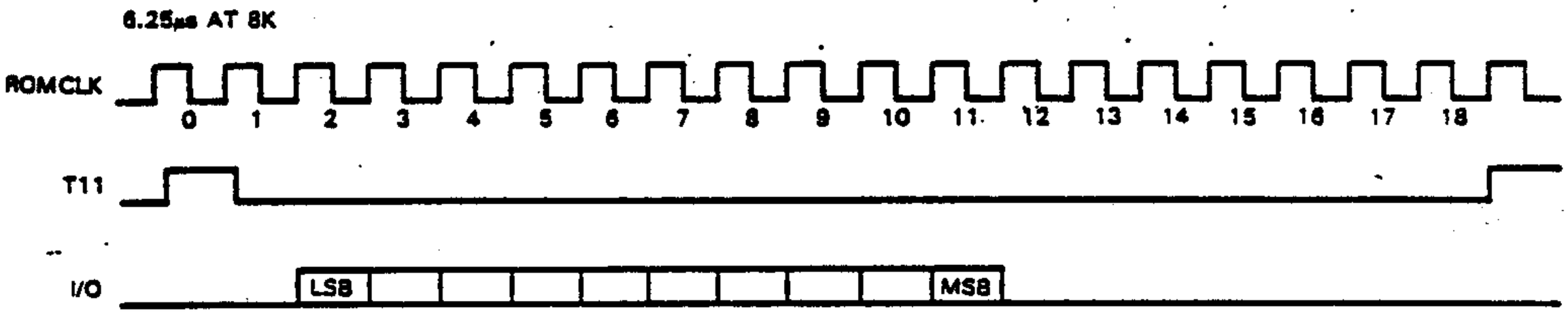


FIGURE 4-4. CIRCUIT FOR ACQUISITION OF 10 BIT BINARY SPEECH DATA

SECTION 5

APPLICATIONS

5.1 MICRPROCESSOR INTERFACE

Although the TMS5220C is operated under the host's control, the VSP does not require full-time supervision. The host controller merely issues macro commands and possibly inputs data. Then the synthesizer takes over and carries out its synthesizer algorithm internally with the data provided from external ROMs, as directed by lines ADD1 through ADD8, M0 and M1, and ROMCLK, much as any other dedicated attached processor would. The following diagram demonstrates a typical interface with a host microprocessor system and an EPROM to control the voice-synthesis processor.

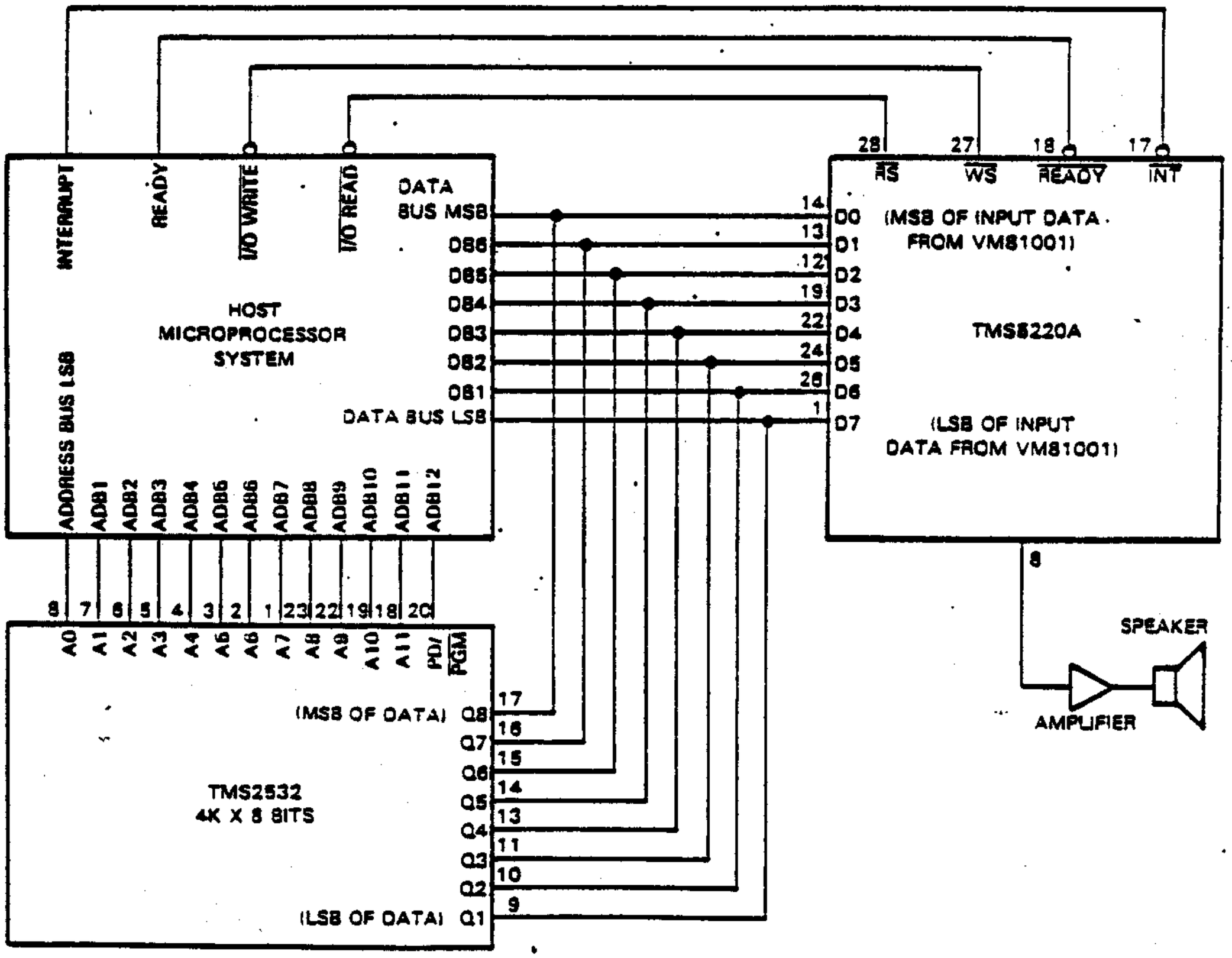


FIGURE 5-1. 5220C INTERFACE WITH HOST COMPUTER

The microprocessor interface is further demonstrated with the following diagram showing TI's TMS 9995 microprocessor system. The 9995's 8-bit data bus is seperate from the microcontroller's 16-bit address bus; hence, no demultiplexing is required to interface the 5220C (and its EPROM), which can simply plug into the 9995's 8-bit data bus. Moreover, the barest amount of logic completes the hardware interface-just two TTL gates and two inverters. The gates develop the required RS and WS inputs to the 5220C from the 9995" WRITE ENABLE outputs. One inverter inverts the 5220C's RDY to the 9995's Memory Ready; the other inverter feeds the WS gate's input from D0 on the data bus.

The software required to add speech to a 9995-based programmable microsystem is as simple as the hardware. By treating the 5220C merely as a memory-mapped device, only one instruction-Move Byte-is necessary to handle all the required signal processing: The Memory Ready input to the 9995 implements the memory mapping of the 5220C and its associated EPROM.

5.2 MICROCOMPUTER INTERFACE

Interfacing to a 5220C chip is slightly more complex when the controller is a microcomputer rather than a microprocessor. Using a microcomputer is tempting because of its on-chip features, such as RAM, ROM, timers, and I/O capability make many low-cost applications economically feasible. Many 8-bit devices offer significant amounts of on-chip ROM and RAM. But microcomputer chips such as the TMS7000, 7020, and 7040 MLP family, the 8048, the 6801, and many others do not offer a Memory Ready input function like the 9995. Still, the lack of a Memory Ready input can be worked around with software. When interfacing micrcomputers, the 5220C should be mapped into the I/O space, which will simplify the hardware. Then, the microcomputer's parallel I/O interface communicates with the VSP's input buffer (FIFOs). In this way the system emulates the memory mapping in software, but the simplified hardware then needs more instructions for operating in the I/O space than in the memory space.

Substituting software for hardware is an excellent tradeoff for low-cost systems whose primary task is speech synthesis. An all-in-one microcomputer- controller/memory can cut an entire speech-synthesizer down to just two chips: the micro and the synthesizer. An 8-bit microcomputer such as the TMS7040 (which carries a 4-kbyte ROM for the vocabulary), working with a TMS5220C, can provide a speech-synthesis capability while still offering a powerful instruction set, on-chip RAM, the remainder (after vocabulary storage) of its on-chip 32-kbit ROM, an on-chip interval timer, and extensive I/O capability. This two chip configuration is depicted in Figure 5-3. Note that if there is insufficient on-board memory for vocabulary storage then an optional VSM can be used. For example a general application may call for a standard vocabulary to be stored on board while a specific application vocabulary may be stored in a VSM. This allows for custom application of a portion of the vocabulary.

Use of the internal microcomputer memory limits operation to the speak external mode. Addition of an optional VSM allows for the use of the speak mode or a combination of both modes.

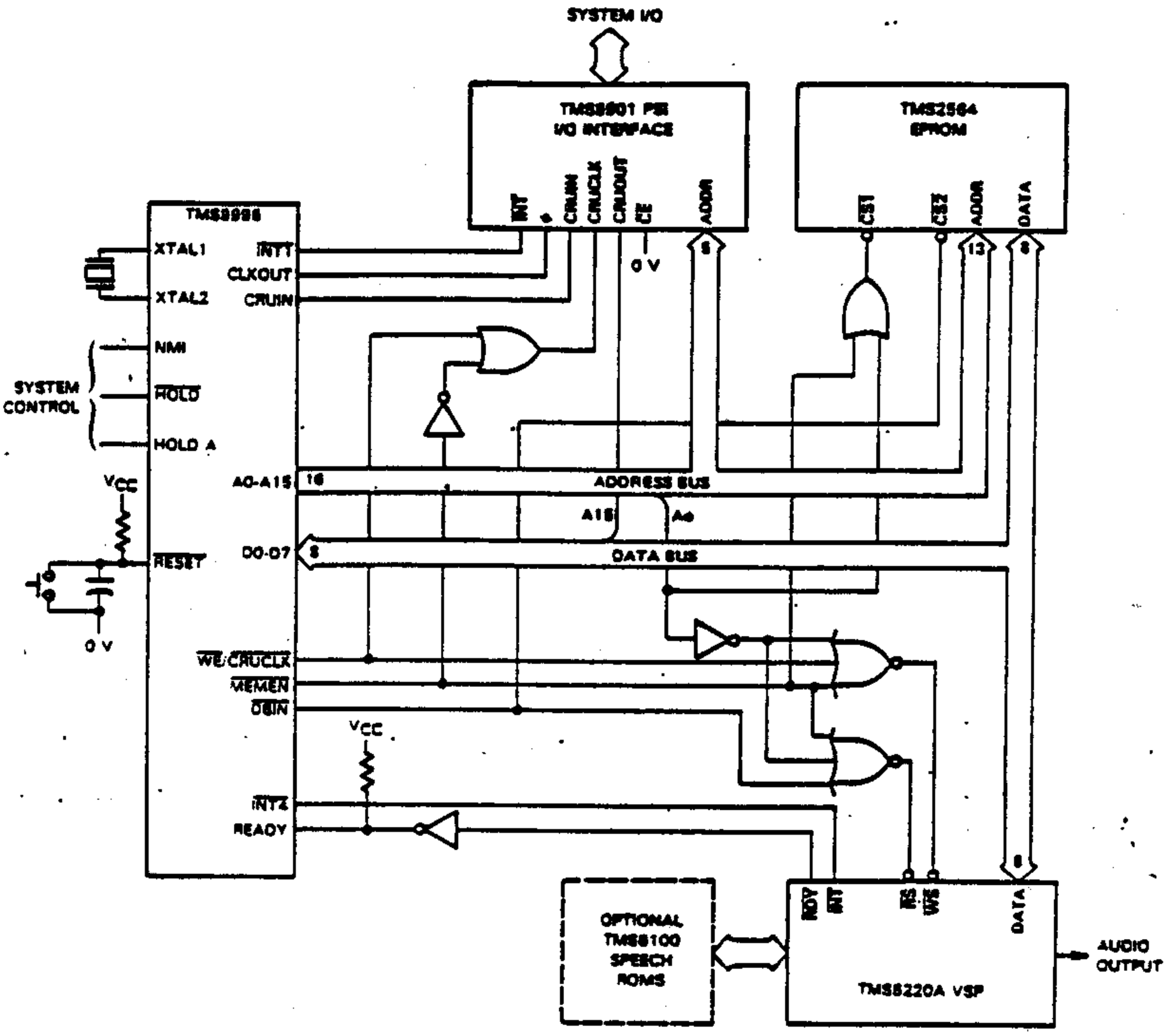


FIGURE 5-2 TMS5220C INTERFACE WITH TMS9995

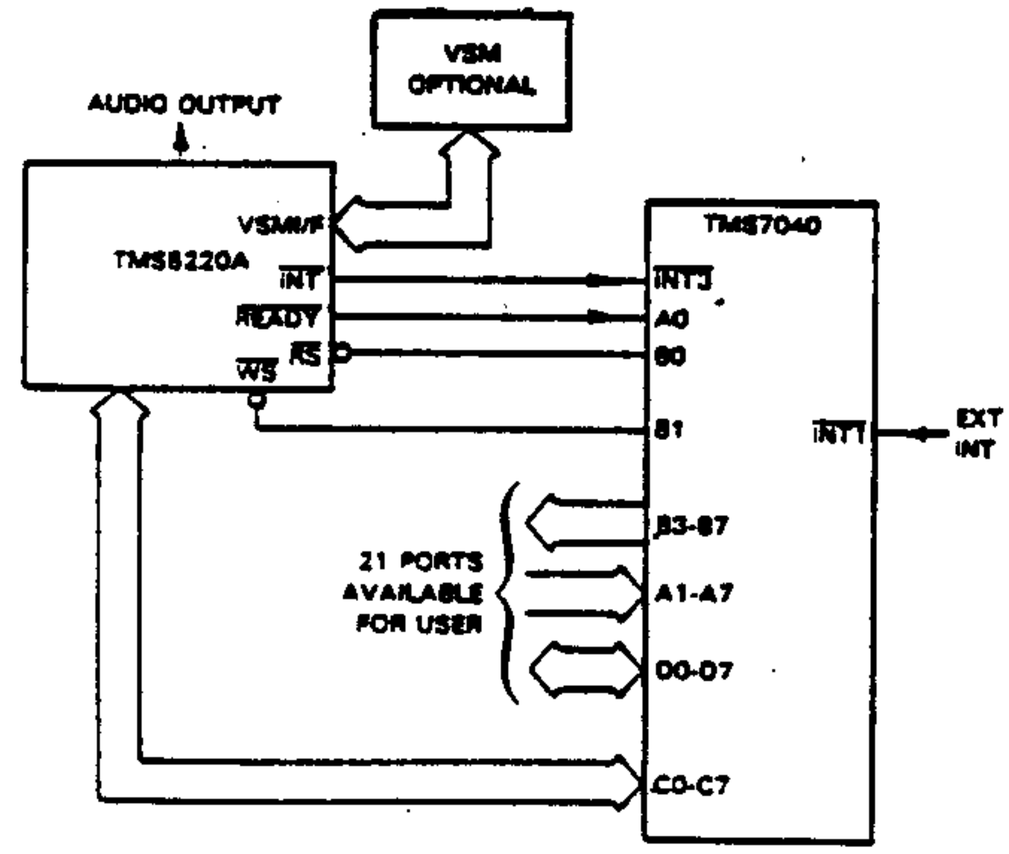


FIGURE 5-3. TWO CHIP SPEECH SYNTHESIS

Since just the first 11 ports of the 7040 peripheral file are hardware-defined for the 5220C, the 7040 can still employ the other 21 ports normally-for example when used for an external keyboard. Thus, the 7040 can communicate with an 8-bit speech-synthesizer chip such as the 5220C, yet maintain substantial processing power.

More memory (or more peripheral devices) can be added to such a basic two-chip system by changing to a memory (or Peripheral) exansion mode of operation. But in a memory-expansion (or peripheral-device) mode, microcomputers fall short. Microcomputers lack the logic needed for block or DMA-type data transfers. They also lack a Memory Ready input for synchronization; accordingly, a microcomputer cannot generate appropriate wait states for the 5220C, which operates much slower than the microcomputers memory cycle.

A TTL octalbus-transceiver chip, TI's 74LS646, provides a solution to this synchronization problem. With eight registered-buffered transceiver circuits and multiplexed three-state drivers, the chip allows the 7040 microcomputer or the 5220C synthesizer to send or receive data asynchronously at each device's own rate. The following diagram depicts a typical interface with the TMS7040 and the 74LS646. See Figure 5-4.

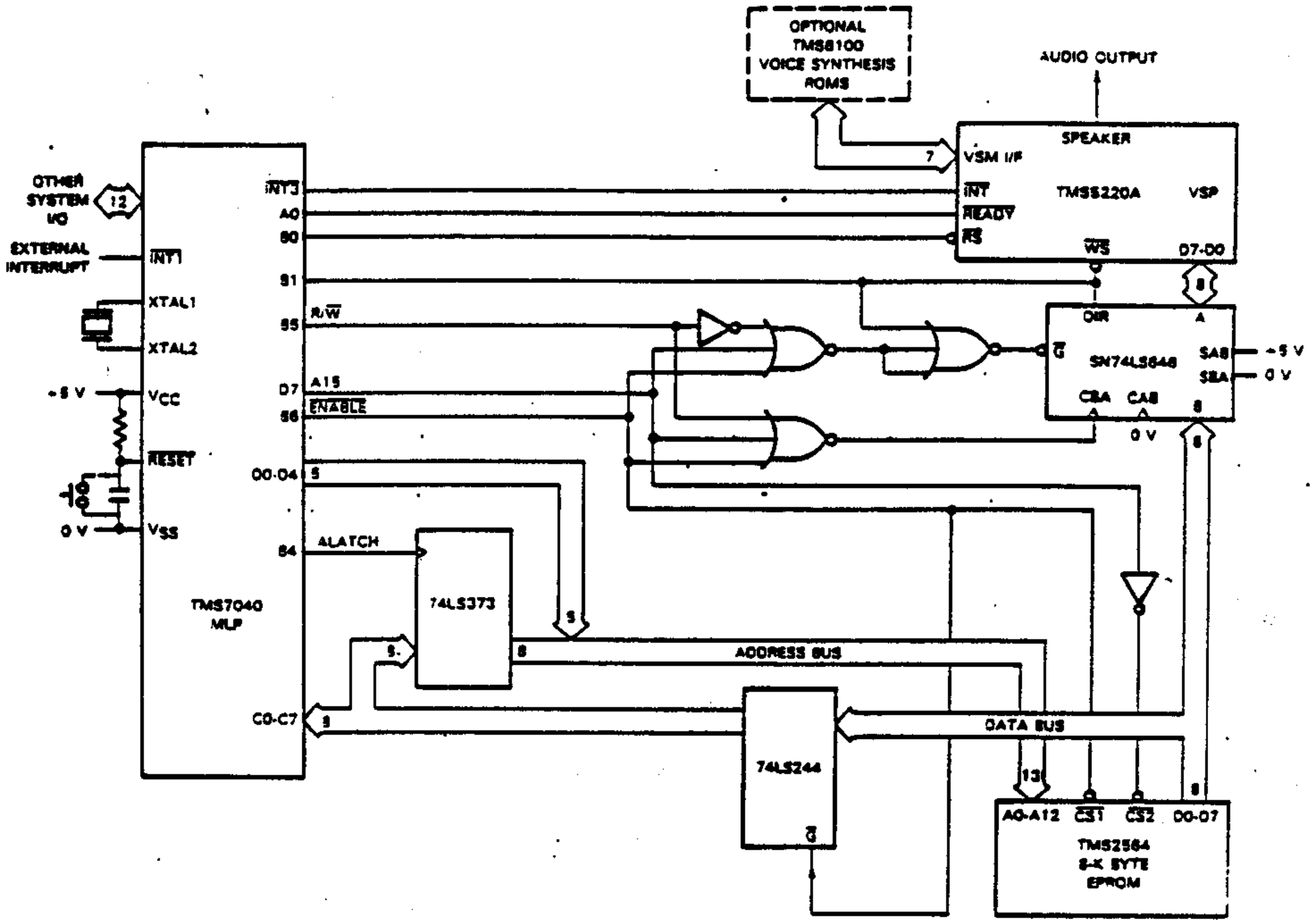


FIGURE 5-4. TMS7040 INTERFACE WITH SN74LS 646

SECTION 6

ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Any pin with respect to V_{SS}	−20 V to +0.3 V
Power Dissipation	600 mW
Operating temperature range	0°C to 70°C
Storage temperature range	−40°C to 70°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{SS}	4.75	5	5.25	V
Supply voltage, V_{REF}		0		V
Supply voltage, V_{DD}	−4.75	−5	−5.25	V
High-level input voltage, V_{IH} (see note 2)	V_{SS}−0.8		V_{SS}	V
Low-level input voltage, V_{IL} (see Note 1)	V_{DD}	0	V_{SS}−4	V
Operating free-air temperature, T_A	0		70	°C
Operational frequency (External RC)	620		625	kHz

NOTE 1: The algebraic convention, where the more-positive (less-negative) limit is designated as maximum, is used in this data sheet for logic voltages levels only.

NOTE 2: Pull up resistors are provided on all data and select inputs. This permits direct drive from TTL compatible devices.

6.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER			MIN	TYP	MAX	UNIT
V_{OH}	D0-D7, WS, RS, INT	I_{OH} = 0.4 mA	2.4		V_{SS}	V
	ROMCLK, ADD 1-8, M0, M1	I_{OH} = 100 µA	V_{SS}−0.5		V_{SS}	V
V_{OL}	D0-D7, WS, RS, INT	I_{OL} = 1.6 mA	V_{RSF}−0.5	0	V_{RSF}+0.5	V
	ROMCLK, ADD 1-8, M0, M1	I_{OL} = 100 µA			V_{SS}+4.5	V
I_{REF}	Supply current from V_{REF} (reference to V_{SS})			3	5	mA
I_{DD}	Supply current from V_{DD} (reference to V_{SS})			10	35	mA
C_i	Input capacitance, (except data bus)			15		pF
C_o	Output capacitance, (except data bus)			15		pF
C_{db}	Data bus load capacitance		25		300	pF

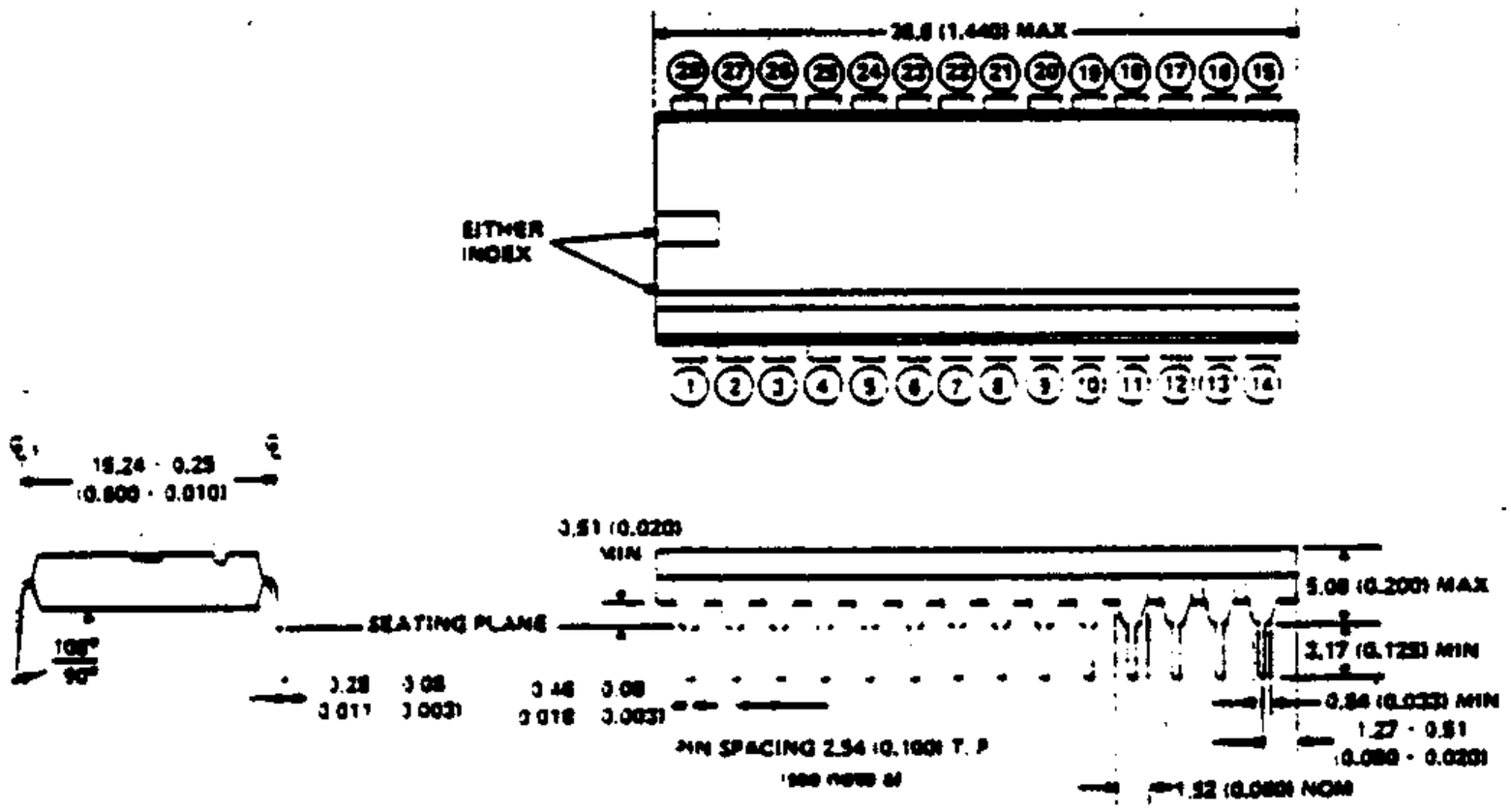
6.4 STATIC DISCHARGE PROTECTION

All inputs and outputs are guarded against electrostatic damage by state-of-the-art protection devices incorporated on the chip.

SECTION 7

MECHANICAL DATA

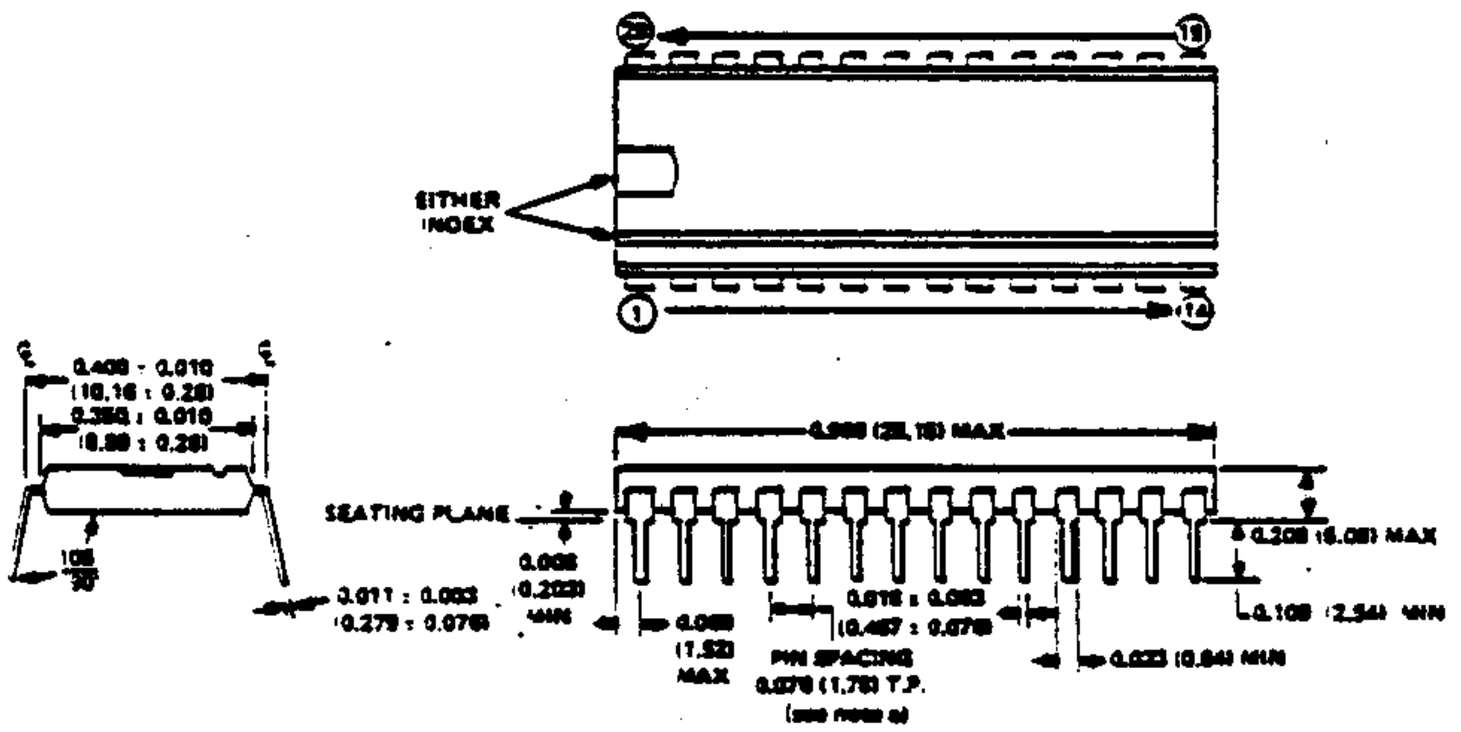
7.1 TMS5220A-28 PIN PLASTIC PAGE. .100" PIN CENTER SPACING, .600" PIN ROW SPACING



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE a: Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.

7.2 TMS5220A-28 PIN PLASTIC PACKAGE, .070" PIN CENTER SPACING, .400" PIN ROW SPACING



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE a: Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.

7.3 ENVIRONMENTAL

TEMPERATURE RANGE

Operating 0° C to 70° C
Storage —40° C to 70° C

HUMIDITY

Operating: 85 percent Relative Humidity at 35° C
Storage: 95 percent Relative Humidity at 55° C.